2011 Int Conf Frontiers of Characterization and Metrology for Nanoelectronics May 25, 2011

Strain Analysis in Scaled Si Transistors by Simulation-Hybrid UV Raman Microscopy

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Supported in part by the MIRAI project, NEDO, Japan.

Requirements for CMOS measurement/characterization

Nanoscale material characterizations are required. •New materials in nanoscale devices results in complicated interfaces. •Variability increases and reliability decreases. CD & LER 30~40 nm Side wall roughness Metal gate Workfunction High-k Material composition, interfacial dipole Source Drain **Dopant distribution** Mechanical Strain Strain distribution

Strain distribution depends on layout.

• Simple physical measurement cannot meet the requirement.

Simulation-Hybrid Stress Measurement



Si

- Ability of polarized UV Raman microspectroscopy in combination with stress simulation and optical simulation
- Strain analysis in scaled Si transistors by stress simulation calibrated with Raman measurements
- Detection of forbidden Raman modes using high-NA optics
- Summary

Visualization of stress distribution by confocal Raman microscope



Spatial resolution



Point spread function of the system

Confocal scanning microscopic image of light scattering by AI dots fabricated with e-beam lithography on SiO₂

→Spatial resolution 120-150nm: diffraction limit

UV Raman scattering (364 nm)

Advantage

- Non-destructive
- Spatial resolution \sim 150 nm
- Small penetration depth \sim 10 nm
- Simulation is feasible

Disadvantage

- Strain/Stress tensor has six components; a single value of Raman shift is insufficient.
- Spatial resolution is not enough.

Polarization dependence analysis with simulation

Polarized Raman measurements in a metal gate structure



Excitation light intensity distribution calculated with FDTD simulation



The light intensity at 5-nm below the Si surface



The stress induced Raman shift for the *aa*-configuration is much larger than that for the cc-configuration

Position (nm)

The stress is localized very close to the gate edge (\sim 50nm) even higher spatial resolution than the diffraction limit of the excitation probe

FEM stress simulation



Polarized UV Raman measurement on (110) surface



Stress distribution in STI on (1-10) cross sectional surface



Raman shift distribution



Stress measurement by polarized UV Raman mapping



Tensile SiN

2D distribution of Raman shift





Calibration using Raman spectroscopy analysis



Structure: nMOSFET with tensile stress liner



Calibration results

Portion	Material	Intrinsic stress (MPa)		Young's modulus (GPa)	Poisson's ratio
		Initial Calibrated			
STI	SiO2	- 220	- 400	72	0.167
Gate	Poly Si	- 500	- 300	145	0.280
Gate, S/D	Silicide	+ 500	+ 700	210	0.329
	Tensile	+ 1550	+ 1250	180	0.286
Stress line	Compressive	- 3450	- 3500	210	0.286

+: tensile

-: compressive

The initial mechanical stress parameters of each material

wafer-bending measurements for intrinsic stress

• nanoindentation measurements for Young's modulus

•the literature on Poisson's ratio.

Structure: pMOSFET with compressive stress liner



Stress distributions calculated by calibrated TCAD



Verification in scaled device by top down Raman measurements

Raman signals only come from under the offset spacer region because the rests of regions are covered with metallic silicide.



FDTD simulation for a gate structure for a-polarization





without side wall









with side wall

SDW dependence measured and calculated Raman shifts



SLX dependence measured and calculated Raman shifts



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High-NA Raman measurement on Si (001) surface



- Polarized UV Raman micro-spectroscopy acquires higher ability to quantitatively analyze local strain by combination with stress simulation and optical simulation.
- Evaluation of mechanical stress in scaled Si MOSFETs using TCAD simulations calibrated by UV Raman measurements.
 - The mechanical stress parameters are calibrated by comparing Raman shift calculated from all tensor components with Raman shifts measured by polarized UV Raman spectroscopy.
 - Calibrated stress simulation agrees with the layout dependence of top-view Raman measurements.