Inelastic Electron Tunneling Spectroscopy for Measuring Microscopic Bonding Structures, Impurities, and Traps

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Acknowledgments:

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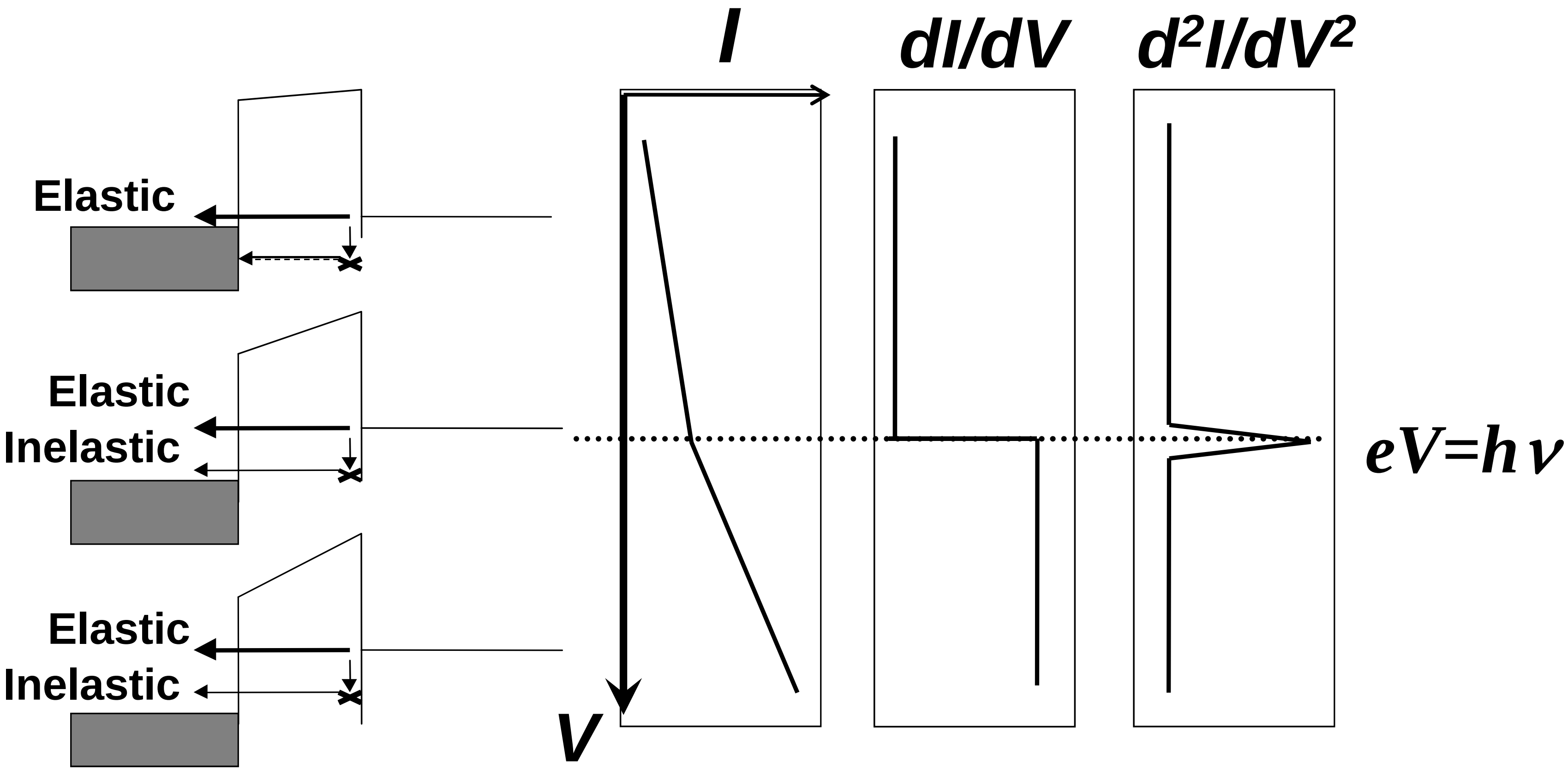
Inelastic Electron Tunneling Spectroscopy

An Inelastic Tunneling Event at E=eV = hν Causes

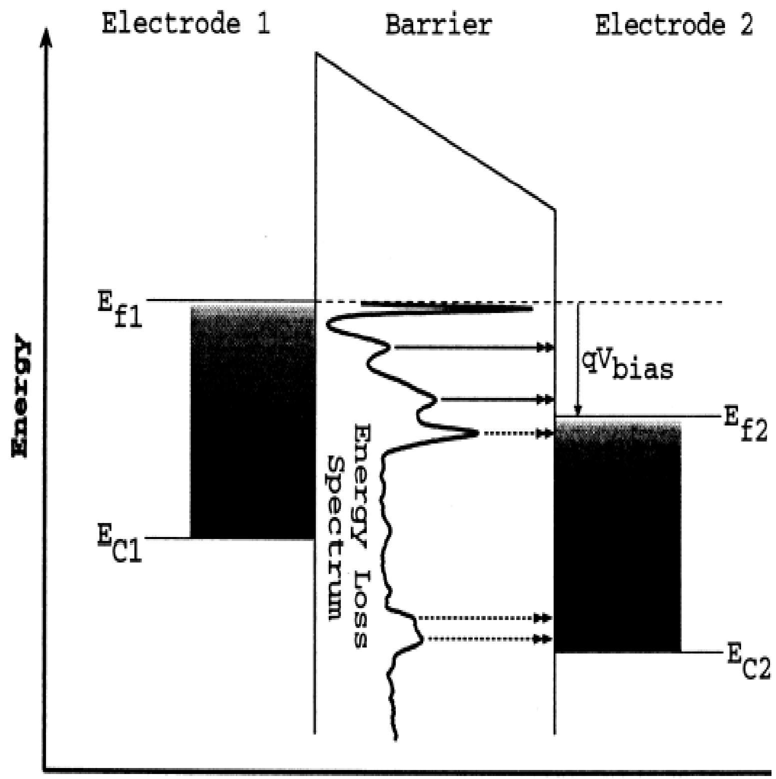
(a) *I-V* to increase slope;

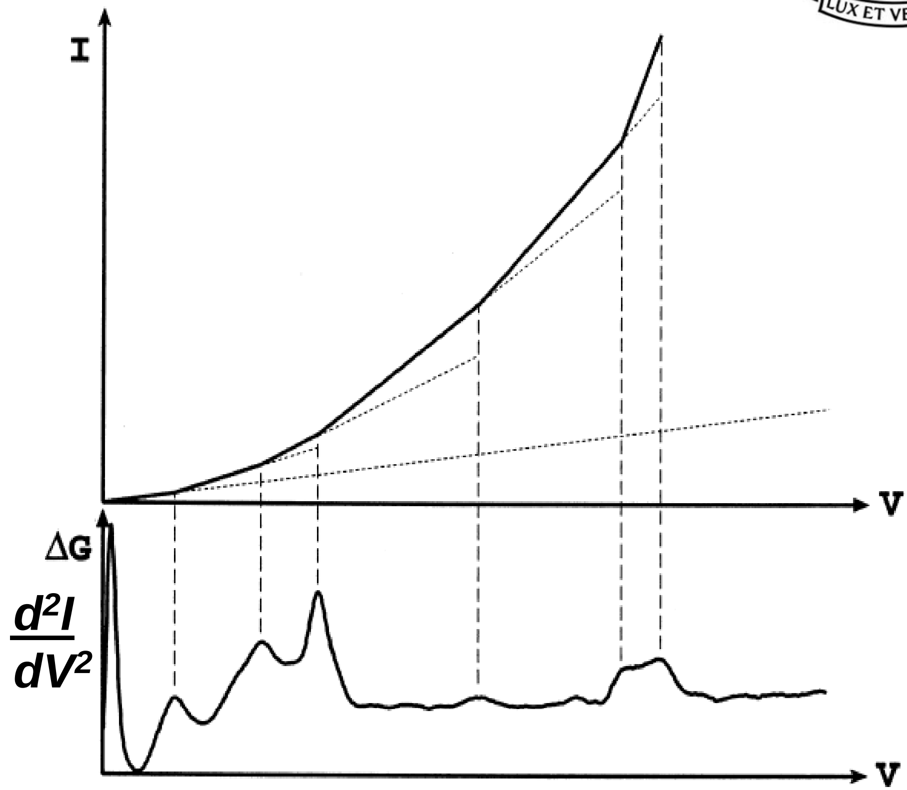
(b) a step in *dI/dV;*

(c) a peak in d^2I/dV^2



Various Inelastic Modes in the Barrier (Left) May Be Reflected in IETS (Bottom Right)



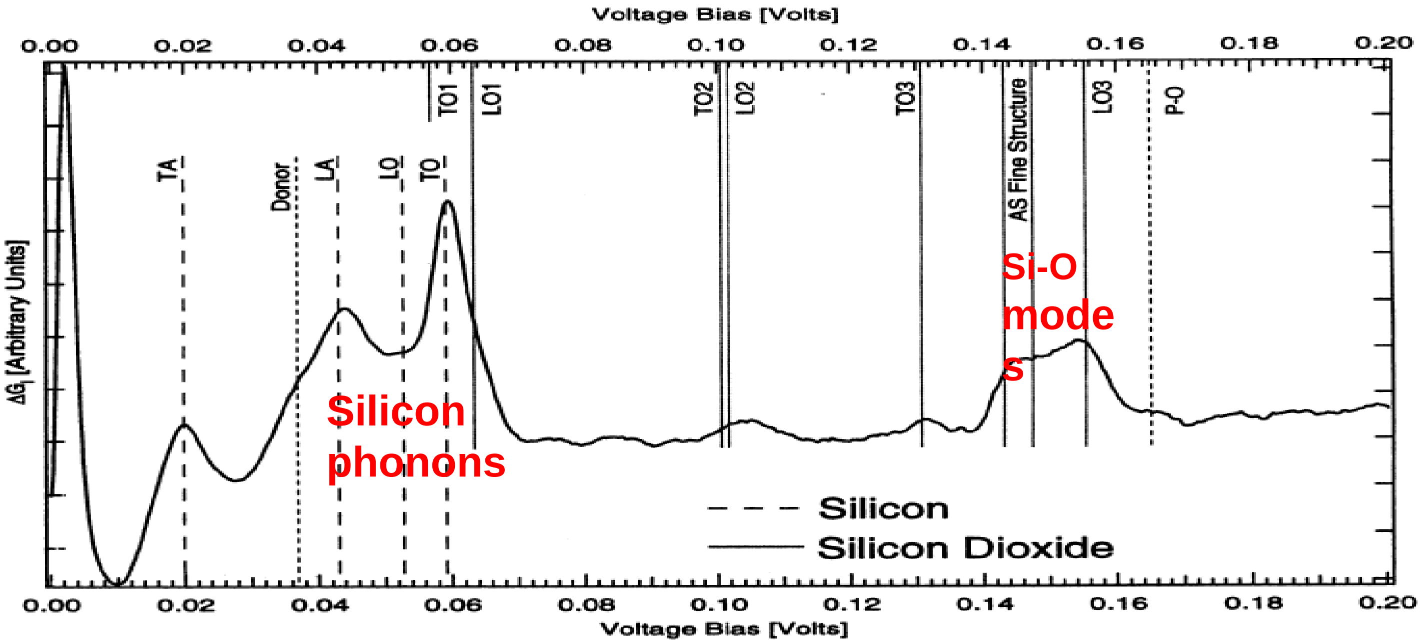


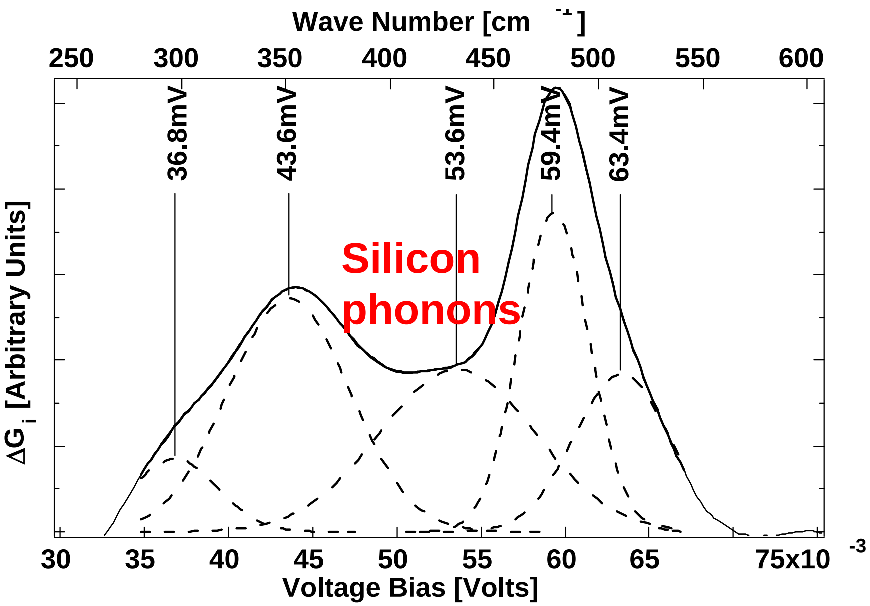
IETS probes phonons, bonding vibrations, impurities, and Traps

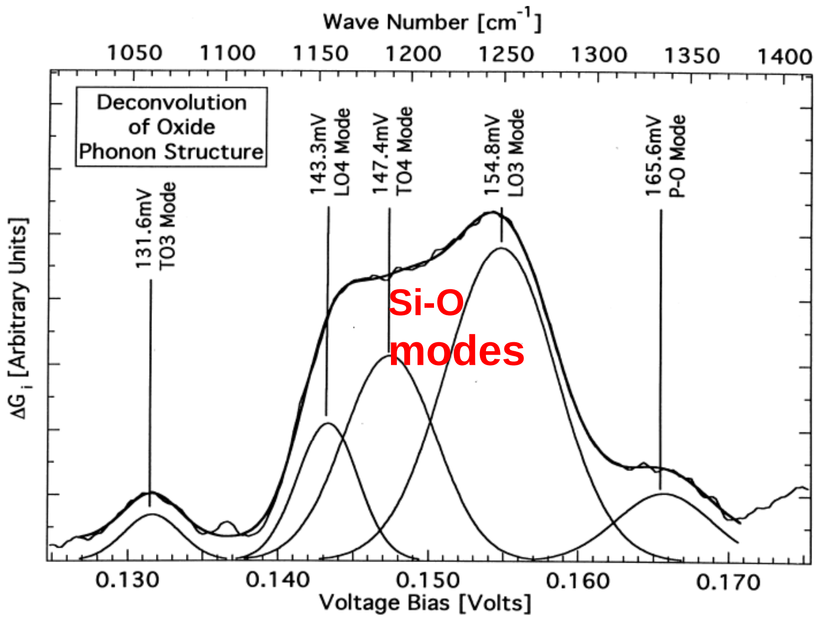
Interactions Detectable by IETS

- Substrate Silicon Phonons
- Gate Electrode Phonons
- Dielectric Vibrations (Phonons)
- Impurity Bonding Vibrations
- Trap States

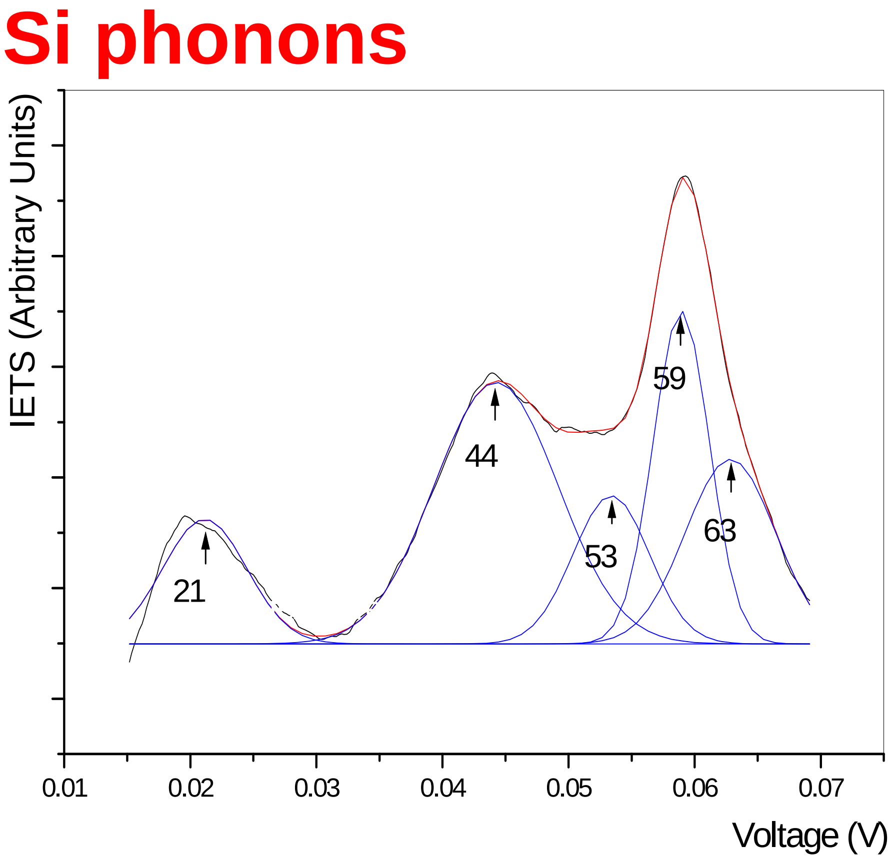
IETS Spectrum of SiO_2/Si

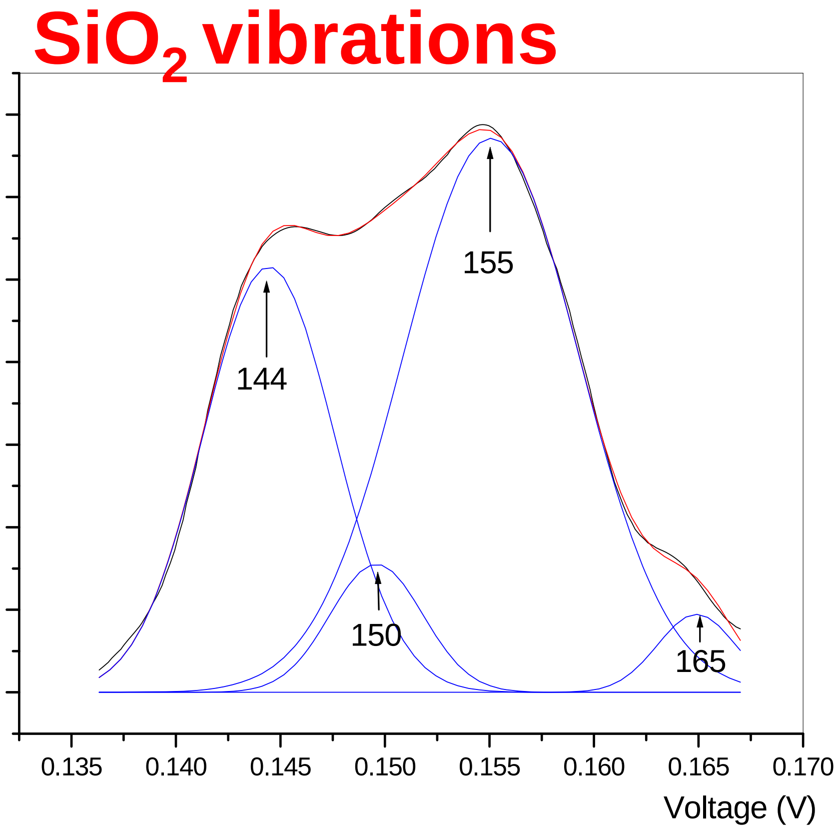






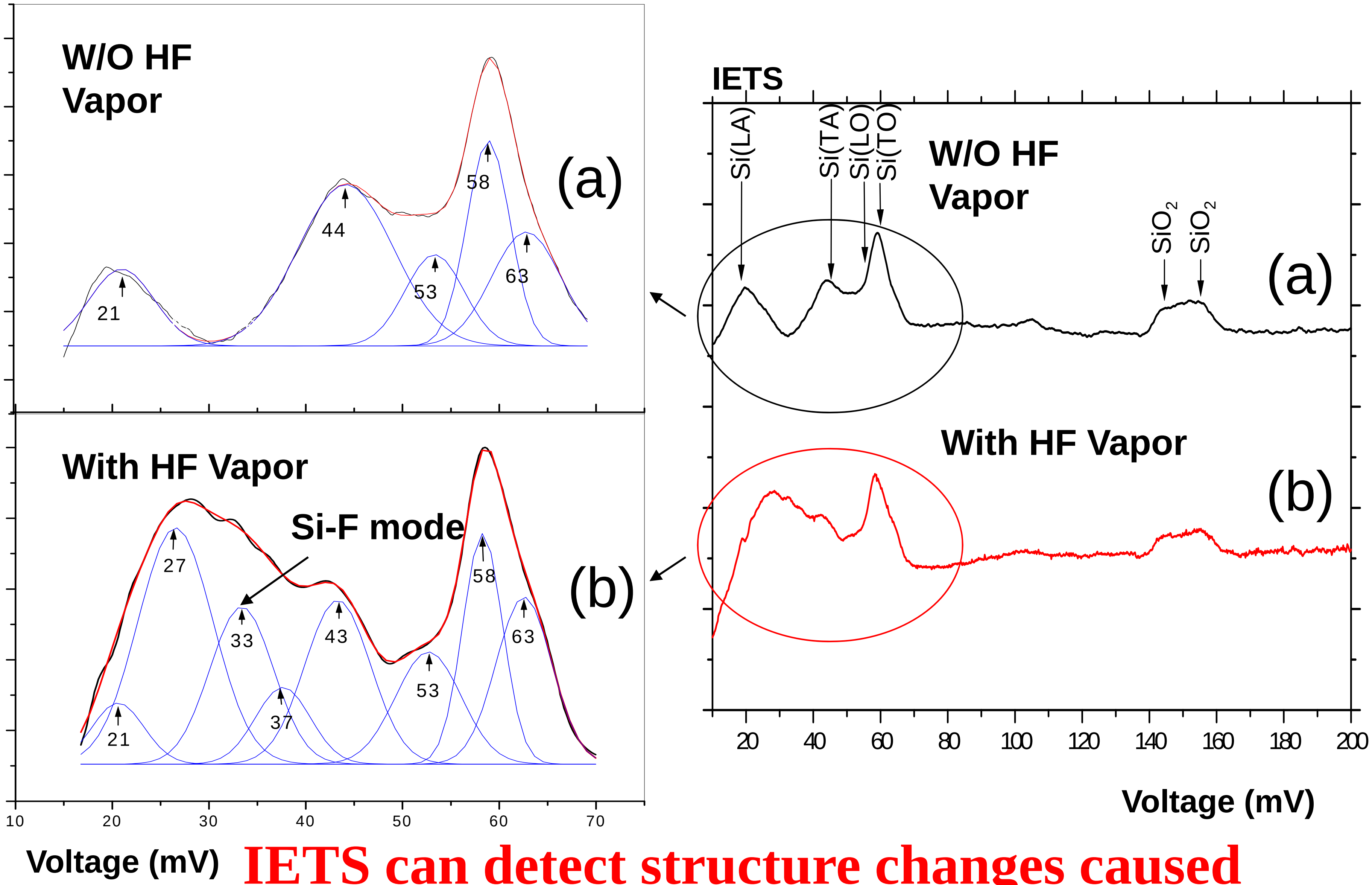
Si phonons and SiO_2 vibration modes





21 mV: Si TA mode
44 mV: Si LA mode
53 mV: Si LO mode
59 mV: Si TO mode

63 mV: Si-O LO1 mode (Rocking)
144 mV: Si-O AS1 mode (Asymmetric Stretch)
150 mV: Si-O AS2 mode (Asymmetric Stretch)
155 mV: Si-O LO3 mode (Symmetrric Stretch)
165 mV: P-O mode

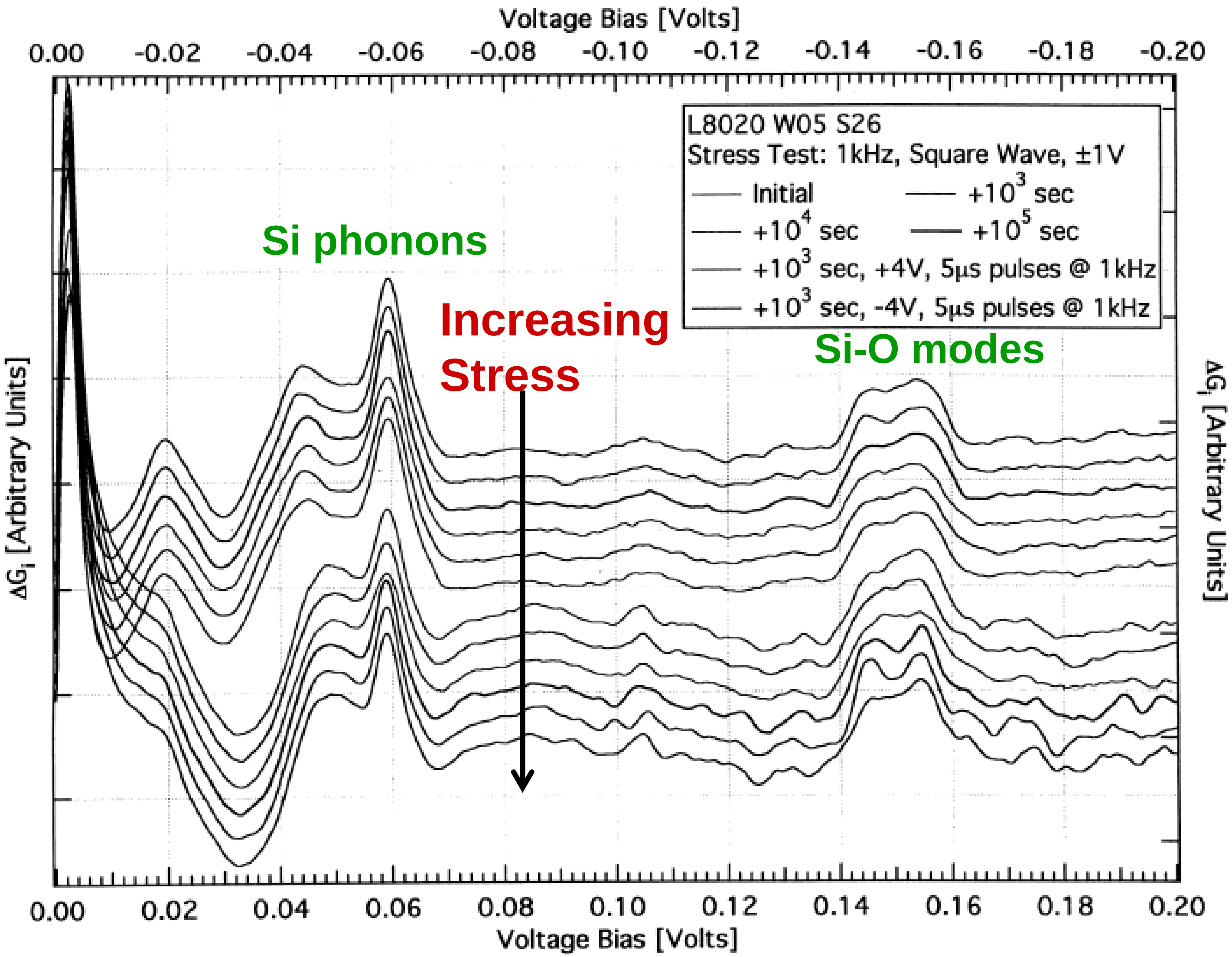


IETS can detect structure changes caused by different processing conditions.

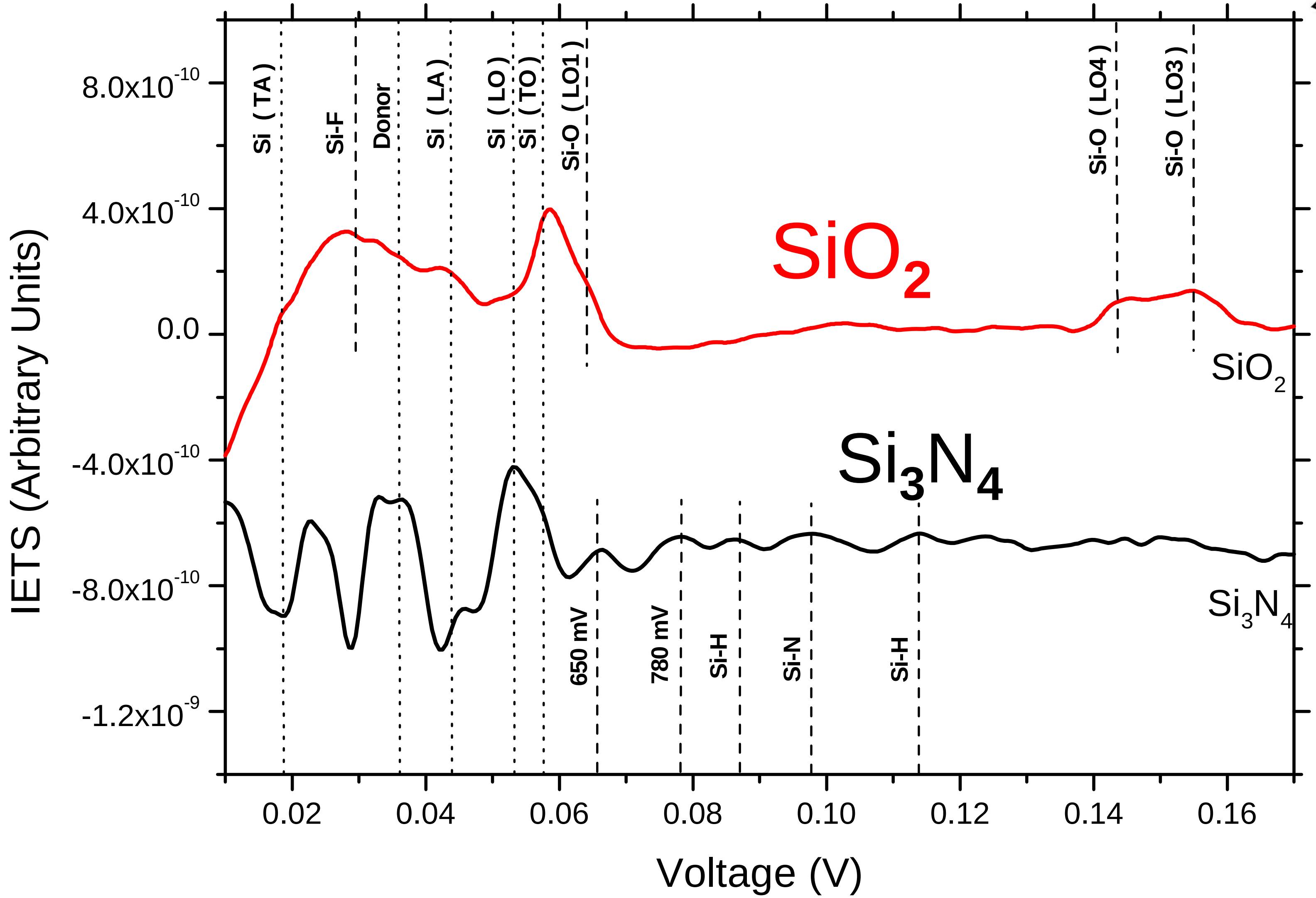
(a) SiO_2/Si without HF vapor pre oxidation cleaning

(b) SiO_2/Si with the HF vapor pre oxidation cleaning

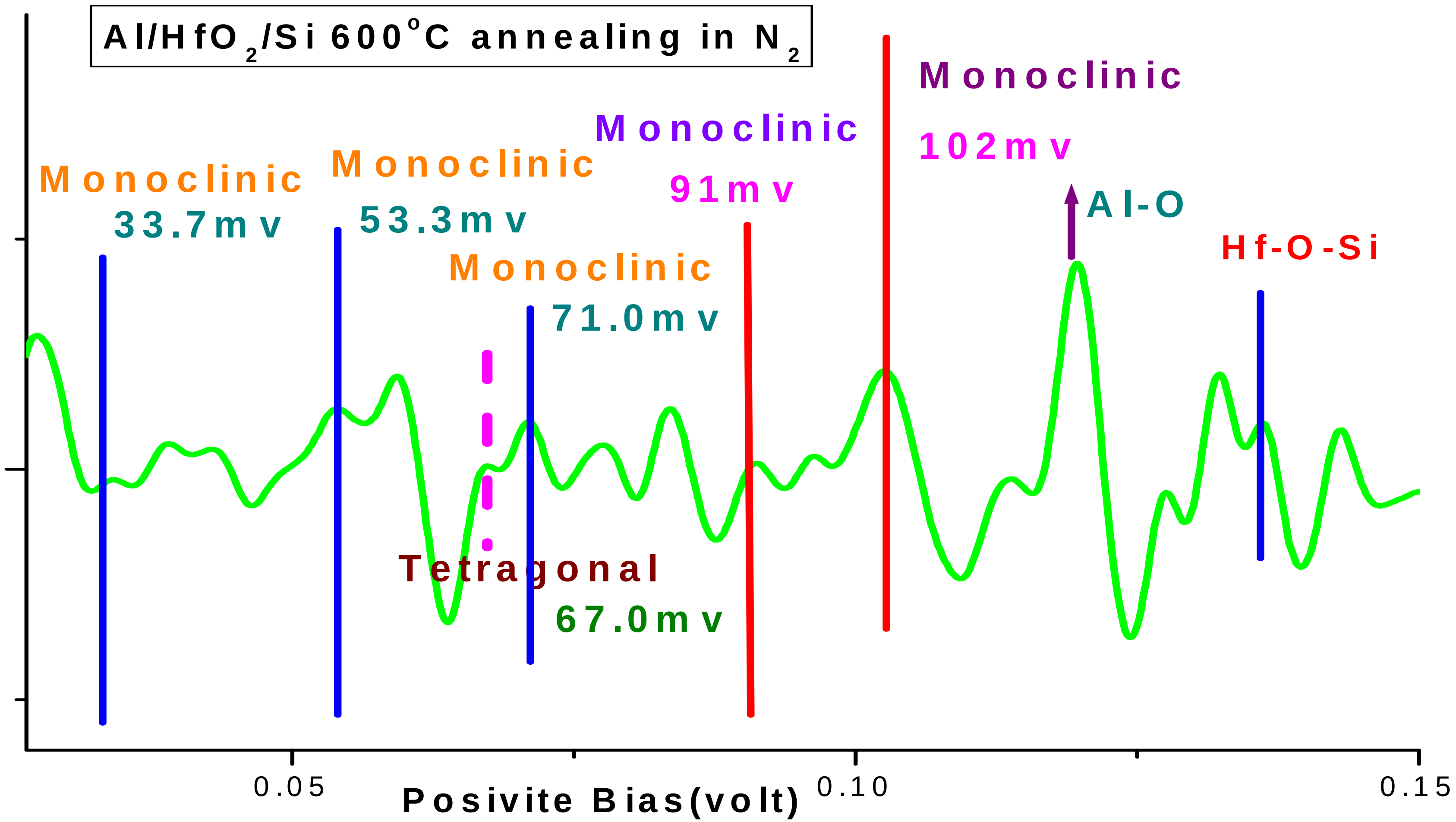
Electrical Stress Alters the Si-O Modes But Leaves the Si Phonons Unchanged



IETS of Thermal SiO_2/Si and CVD Si_3N_4/Si



IETS of Al/HfO$_2$/Si



Remote Phonon Scattering

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Effective electron mobility in Si inversion layers in metal–oxide–semiconductor systems with a high-κ insulator: The role of remote phonon scattering

1

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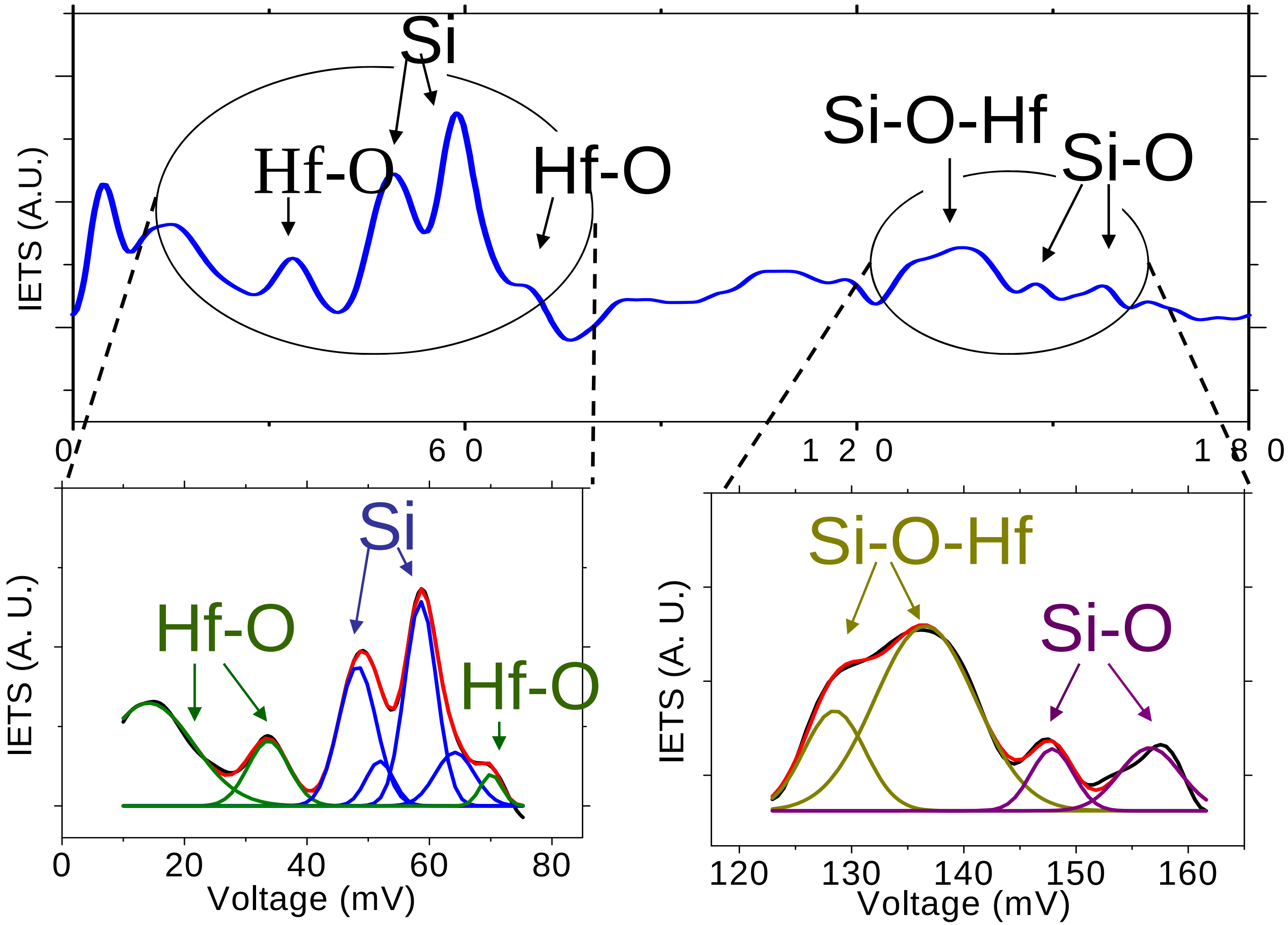
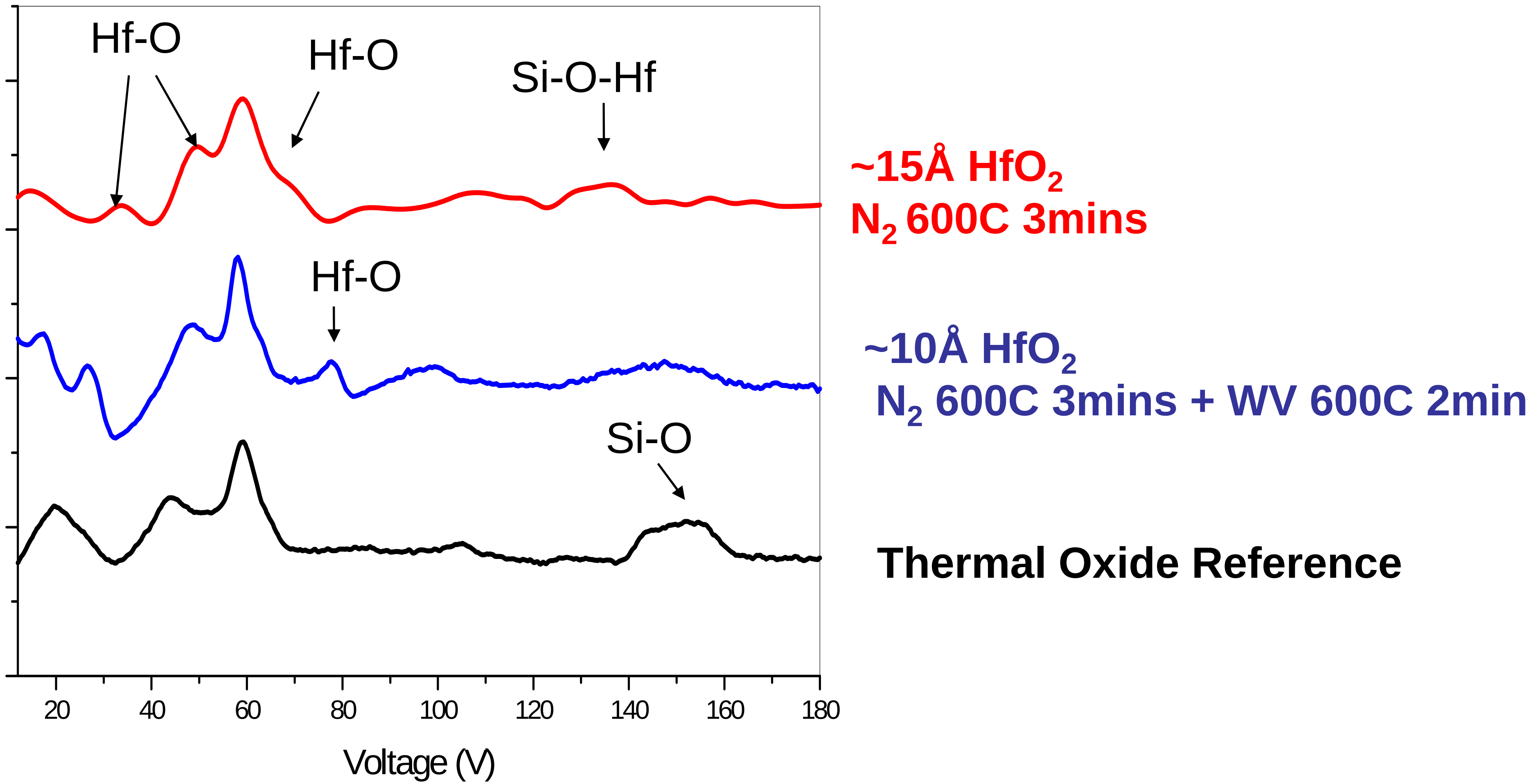
The high dielectric constant of insulators currently investigated as alternatives to SiO_2 in metal–oxide–semiconductor structures is due to their large ionic polarizability. This is usually accompanied by the presence of soft optical phonons. We show that the long-range dipole field associated with the interface excitations resulting from these modes and from their coupling with surface plasmons, while small in the case of SiO_2, for most high-κ materials causes a reduction of the effective electron mobility in the inversion layer of the Si substrate. We study the dispersion of the interfacial coupled phonon-plasmon modes, their electron-scattering strength, and their effect on the electron mobility for Si-gate structures employing films of SiO_2, Al_2O_3, AlN, ZrO_2, HfO_2, and $ZrSiO_4$ for "SiO_2-equivalent" thicknesses ranging from 5 to 0.5 nm. [DOI: 10.1063/1.1405826]

IETS Signals of HfO_2/Si



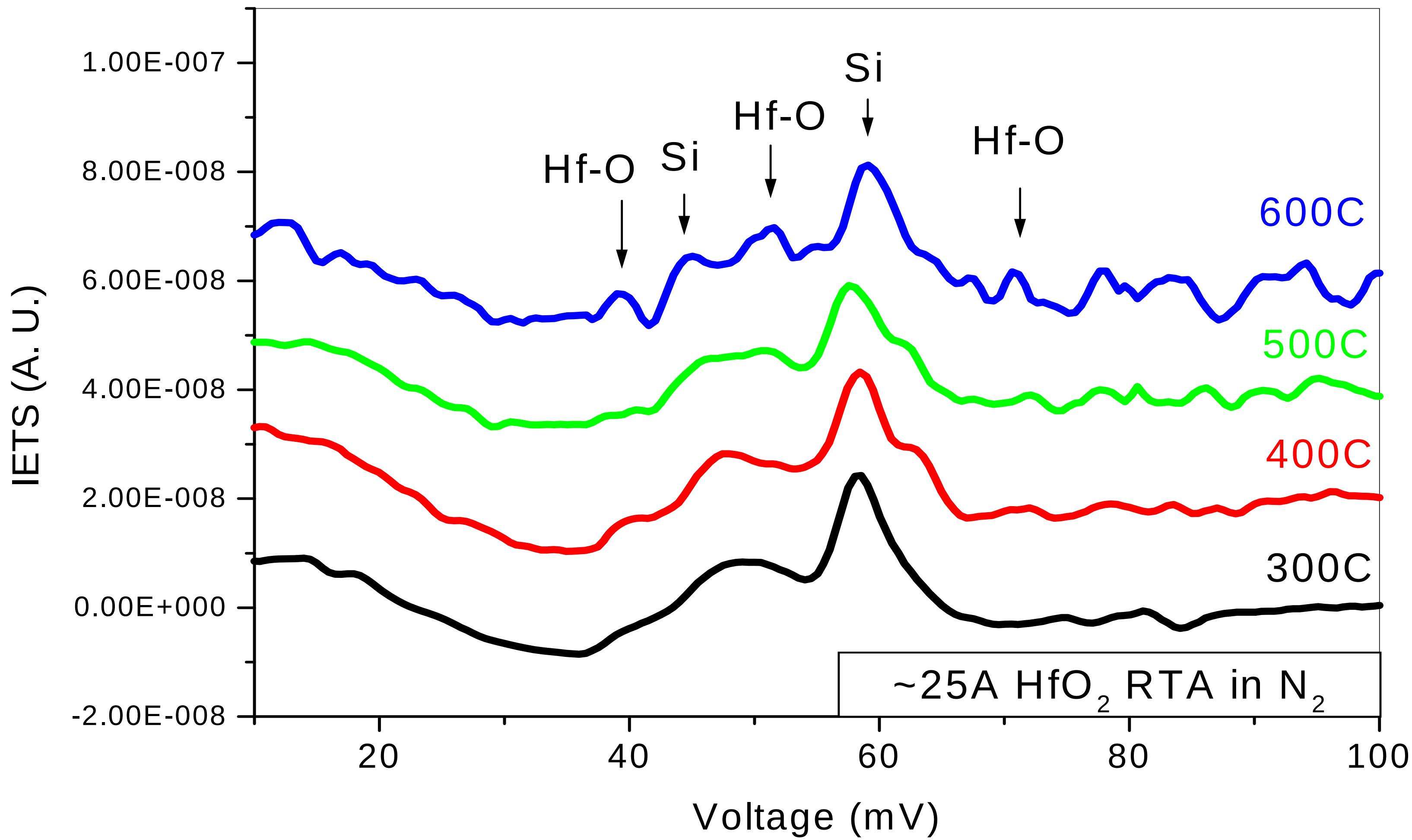
Lower energy peaks are Si and HfO_2 phonons;
Higher energy peaks are Si-O and SiO-Hf phonons

IETS sensitive to process variations for Al/HfO_2/Si structure



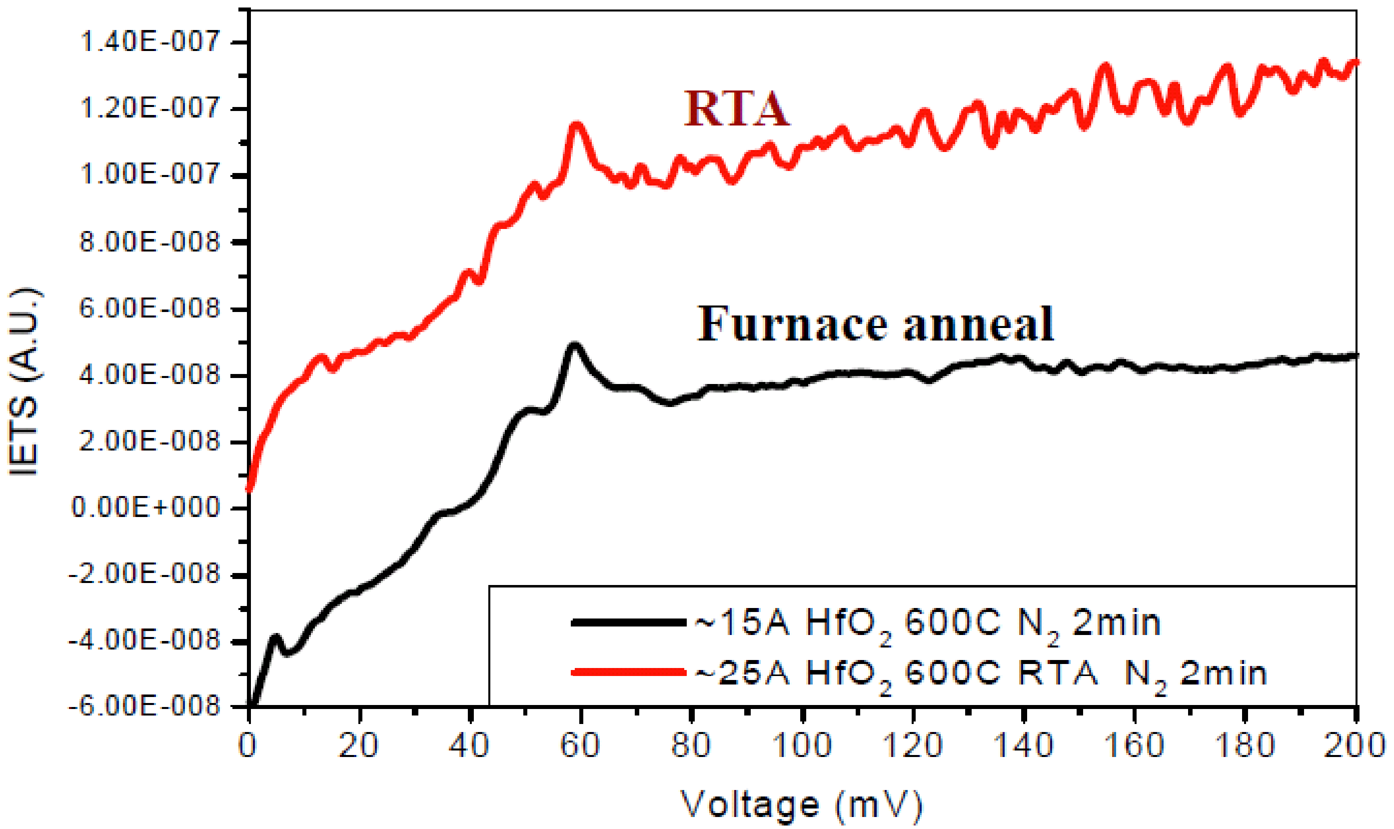
IETS sensitive to process variations for Al/HfO_2/Si structure

- Hf-O peaks stronger with increasing PDA temperature
- More HfO_2 crystallization at higher temperatures.



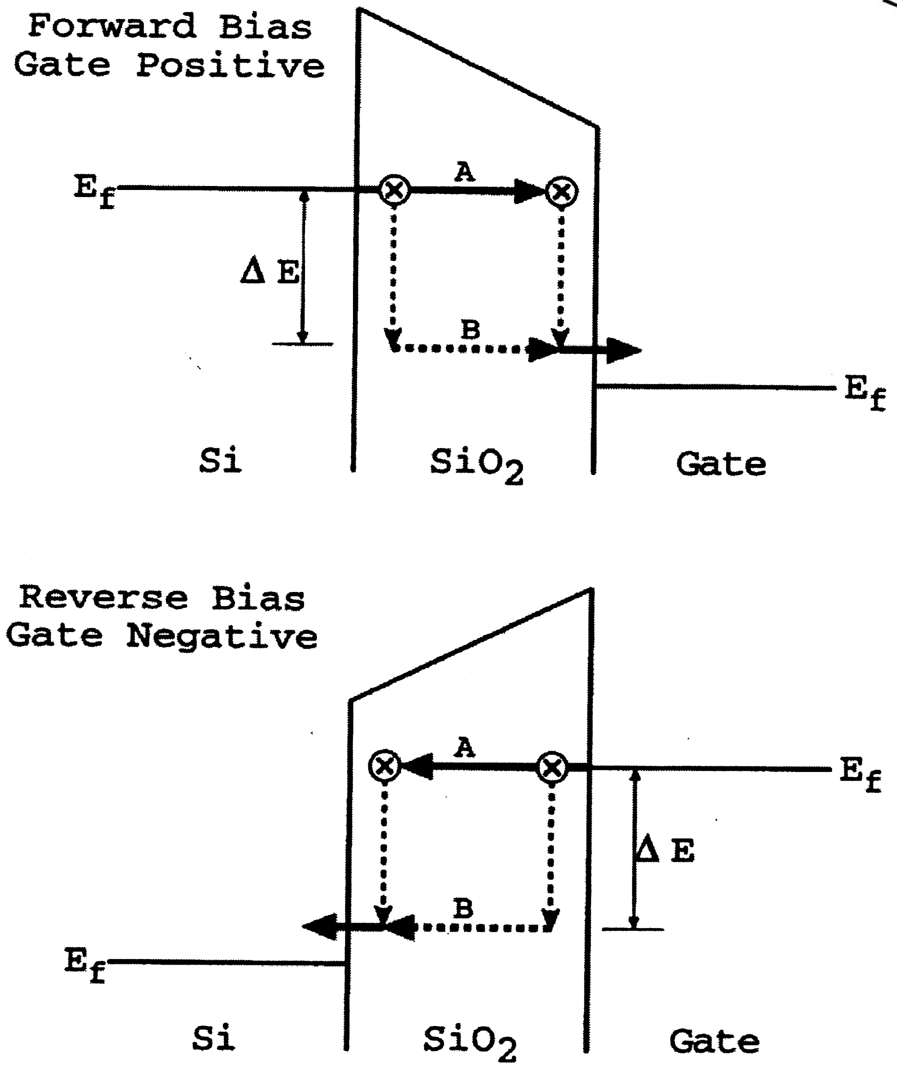
IETS sensitive to process variations for Al/HfO_2/Si structure (1)

Post-deposition annealing: Furnace vs. RTA



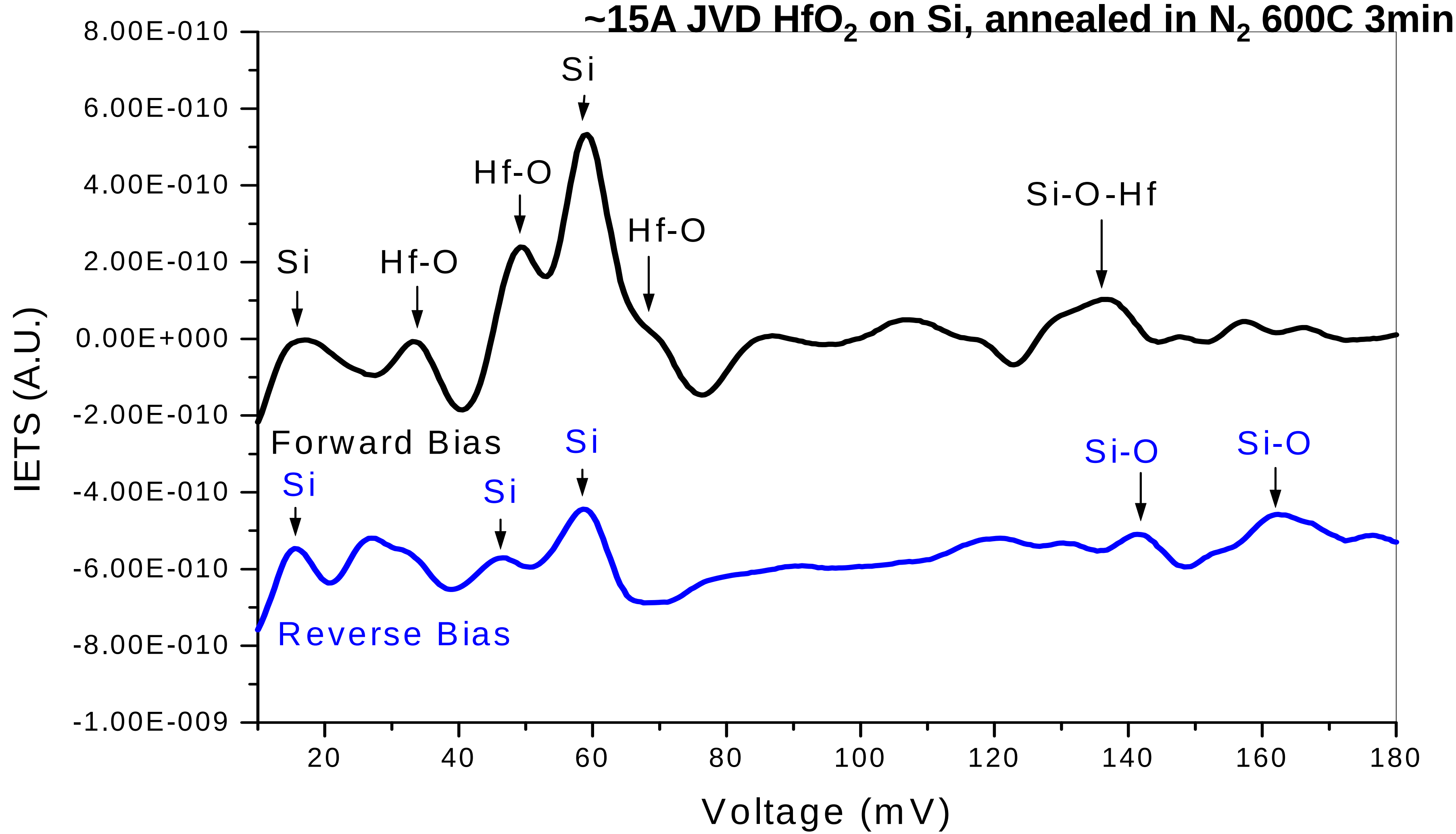
Bias Polarity Dependence

IETS preferentially probes sites near the positively biased electrode



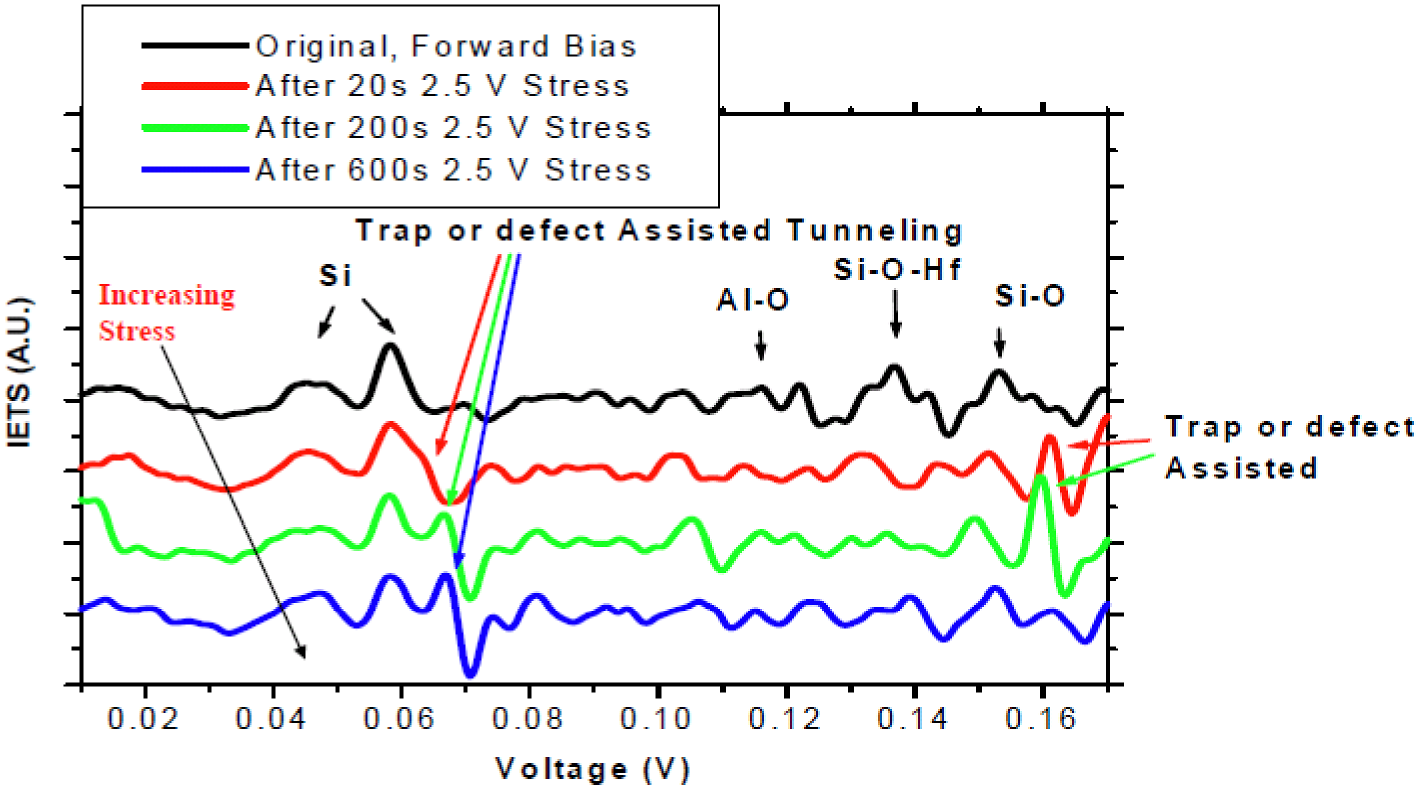
Bias Polarity Dependence of IETS

- Significantly different microstructures near Al-HfO_2 interface and Si-HfO_2 interface.
- HfO_2/Si interface is more SiO_2-like.
- HfO_2/Al interface is more HfO_2-like.

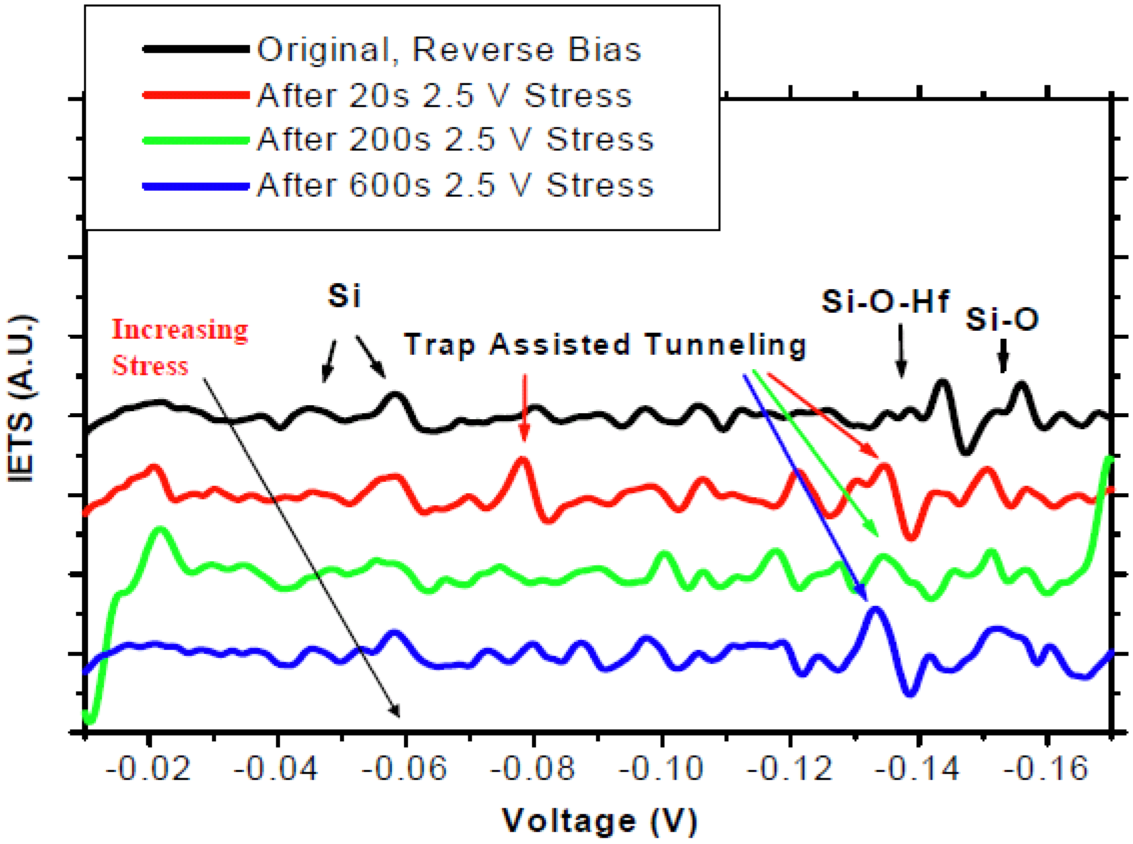


Voltage Stress Induced Effect

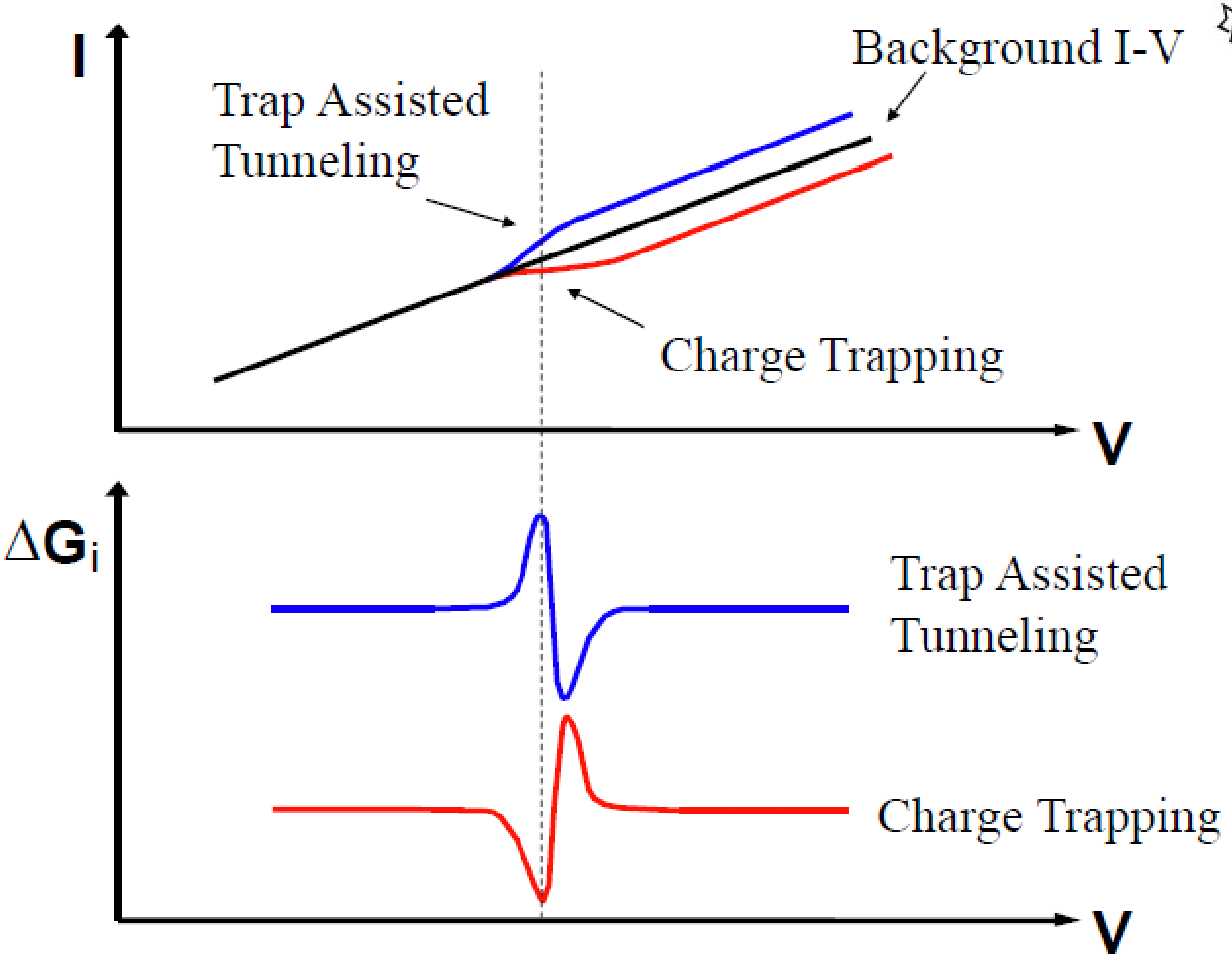
Features at 0.07V and 0.16V indicate trap assisted tunneling.



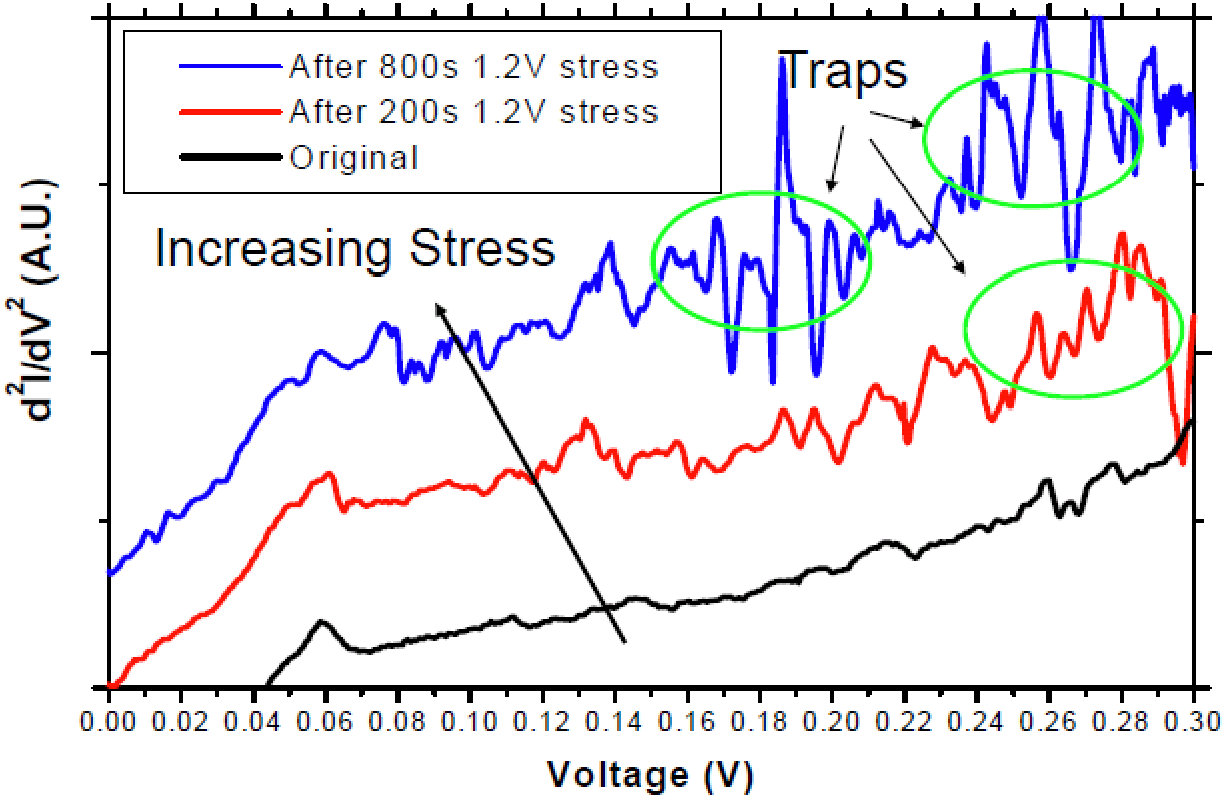
Voltage Stress Induced Effect (Reverse Bias)



Trap Related Effect from IETS

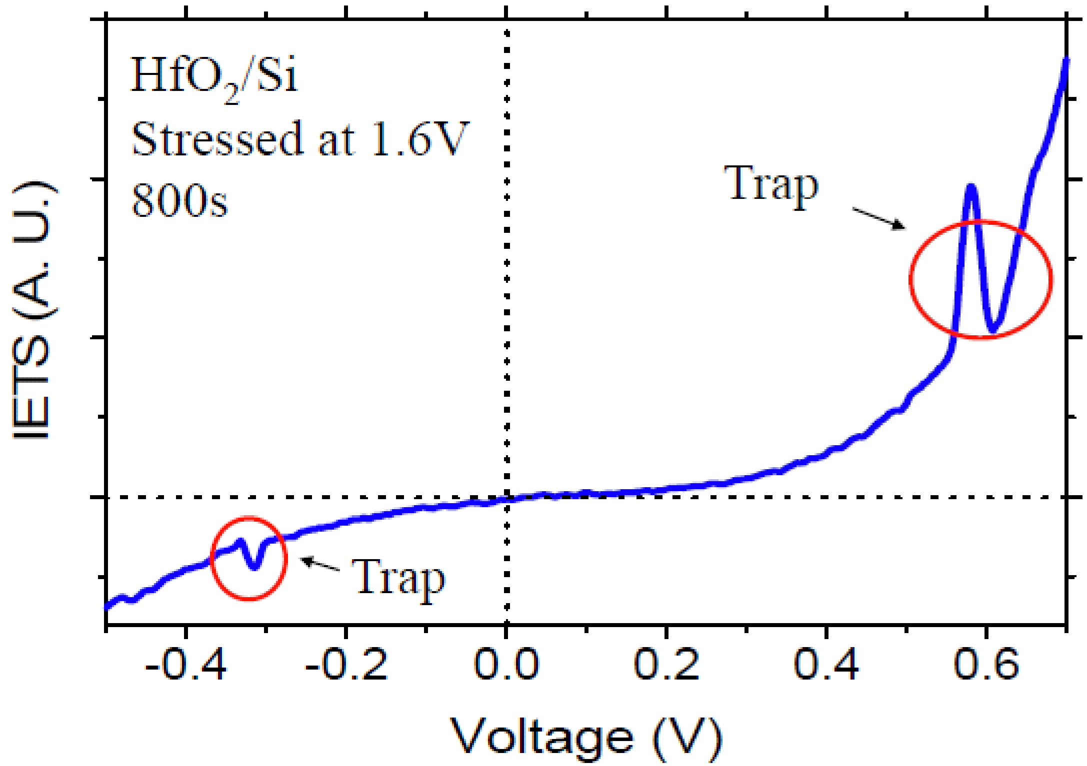


IETS Reveals Stress-Induced Traps



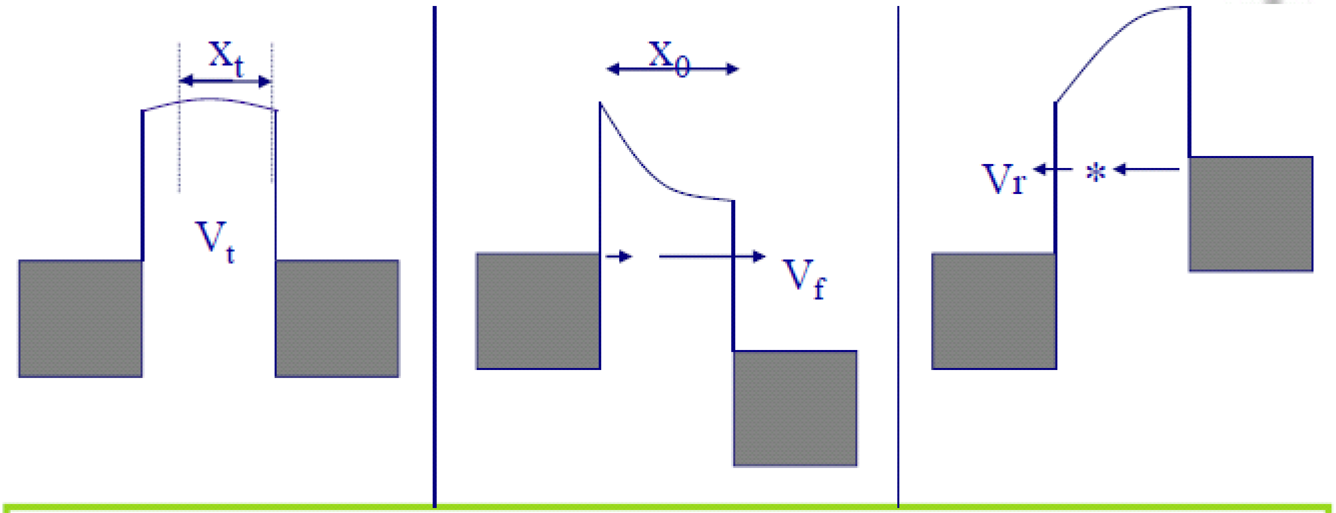
IETS has high sensitivity in detecting traps.

Strong Trap Assisted Tunneling Effect Revealed by IETS



Forward-bias trap features are stronger than reverse-bias ones, due to asymmetry of the barrier.

Determining Trap Energy and its Physical Location from Forward and Reverse IETS



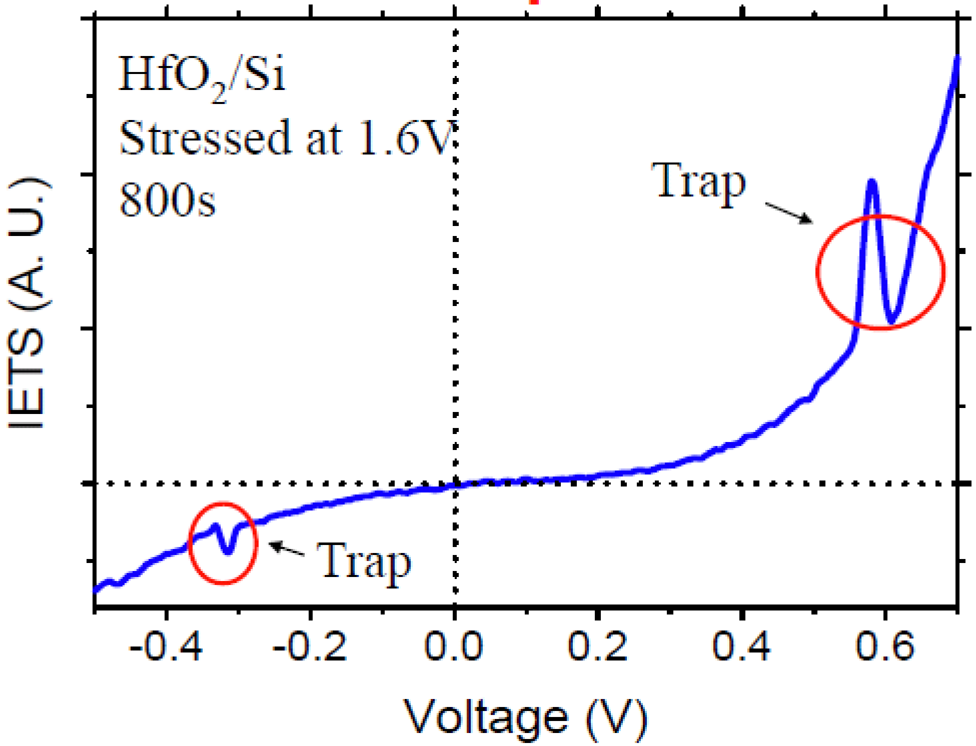
x_t is the physical location of the trap (assume total physical thickness is x_0).
eV_t is the trap energy above the Fermi level (at zero bias).
V_f is the forward bias voltage required for the Fermi level to reach the trap.
V_r is the reverse bias voltage required for the Fermi level to reach the trap.

Assume non-uniform dielectric constant: ε=ε(x).

$$V_t = V_f V_r / (V_f + V_r)$$
$$d_t = d_0 V_f / (V_f + V_r)$$

where $d_0 = \int_0^{x0} dx/\varepsilon(x)$, $d_t = \int_0^{xt} dx/\varepsilon(x)$

Trap Energy and its Physical Location for a Particular Trap



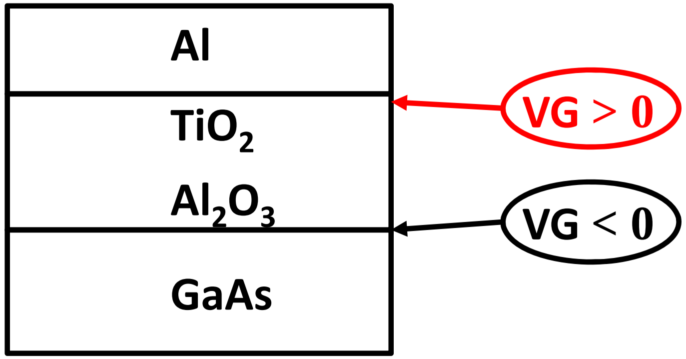
$V_f = 0.58$ V
$V_b = 0.32$ V

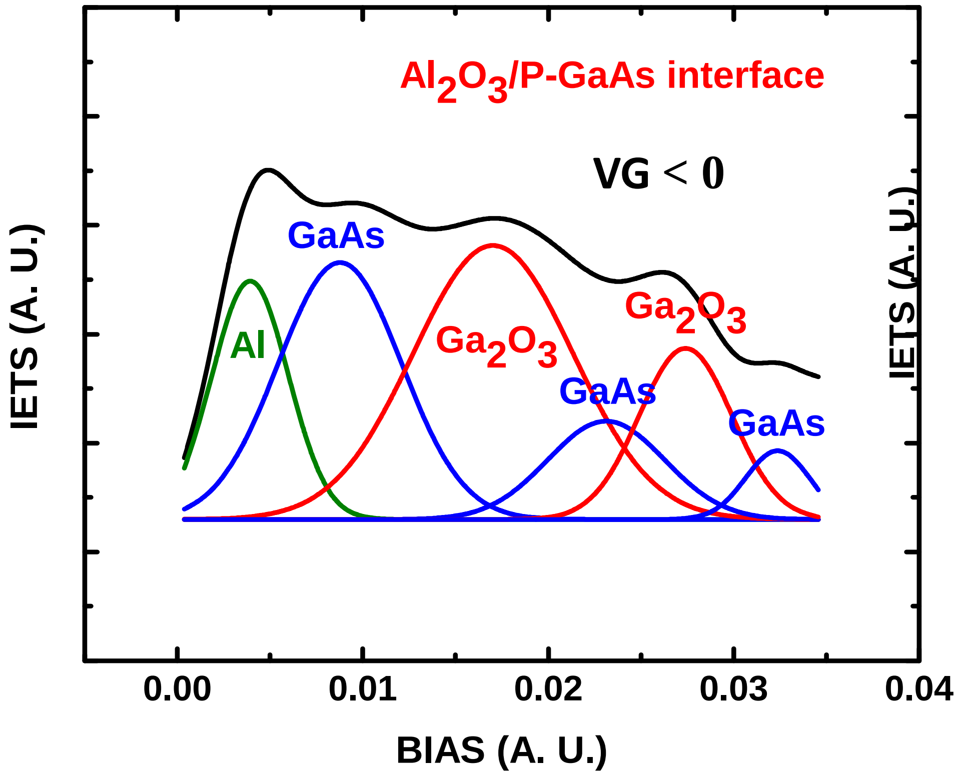
$V_0 = 0.21$ V
d = 0.36

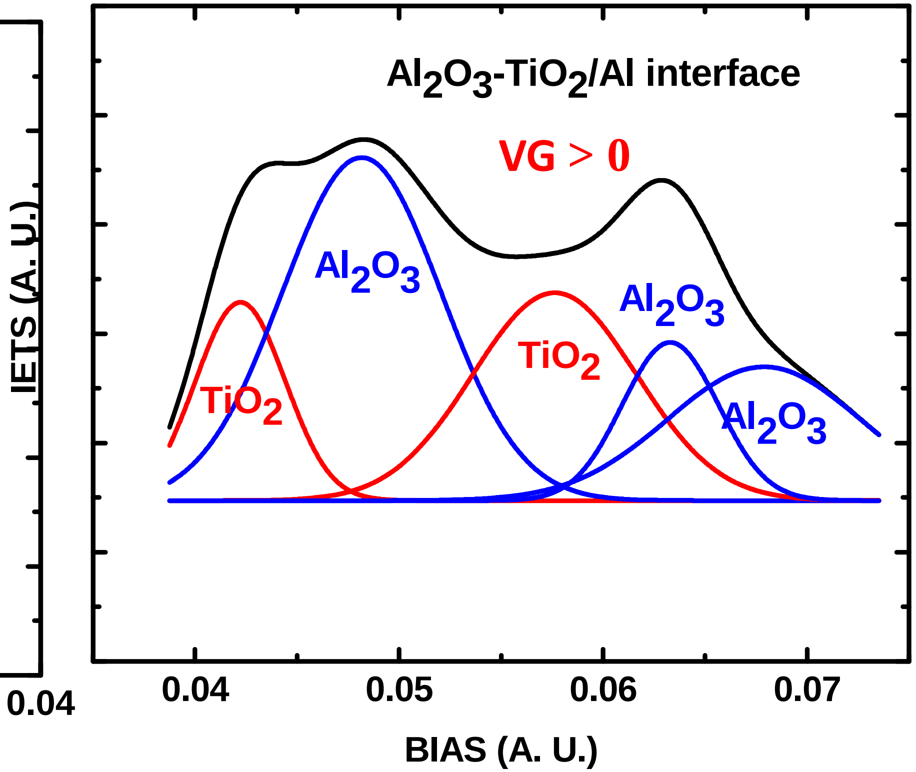
The EOT of the dielectric is ~2.5 nm. ➡ The trap is located ~ 0.9 nm from the dielectric/Si interface

IETS of Gate Stacks on GaAs and InGaAs

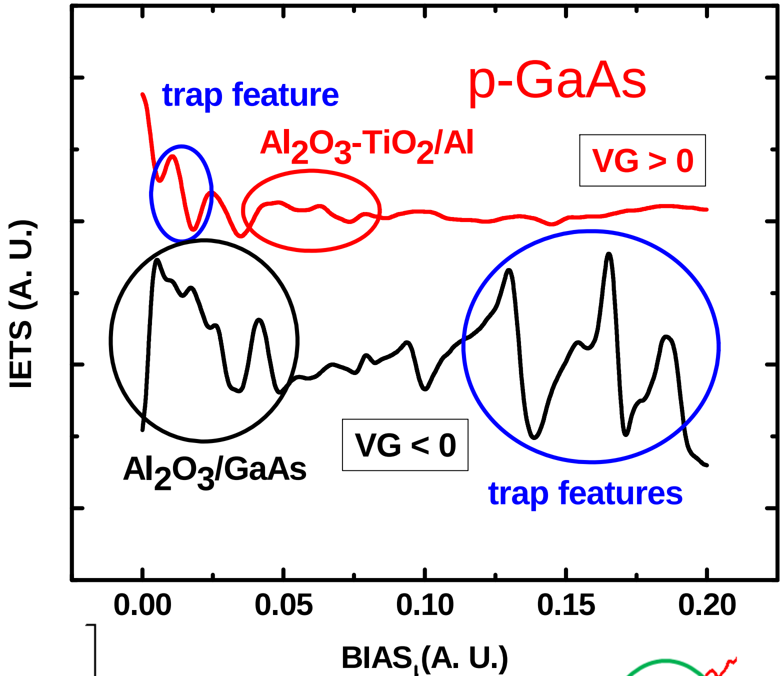
Al/Al2O3-TiO2/GaAs

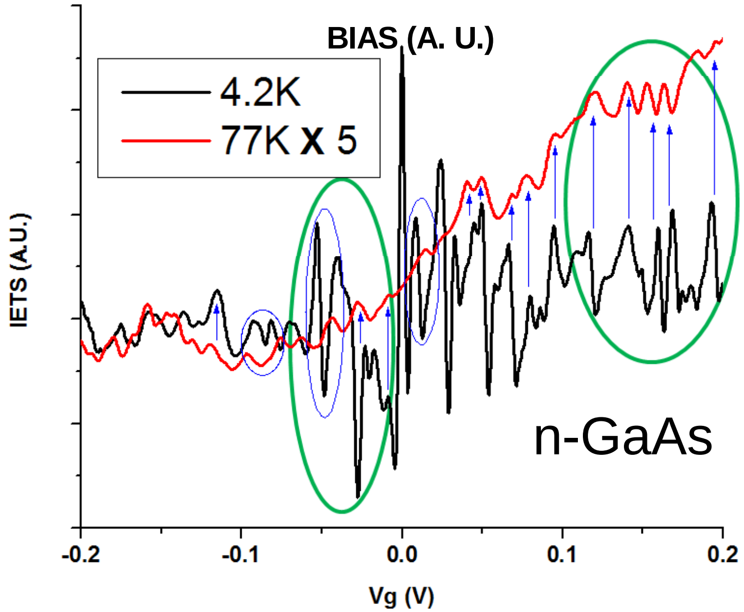






Traps: p-GaAs vs. n-GaAs





p-GaAs MOS:

1. Traps Near Al/TiO_2 (10%·d_0)
2. May be related to Al_2O_3 formation at Al/TiO_2

n-GaAs MOS:

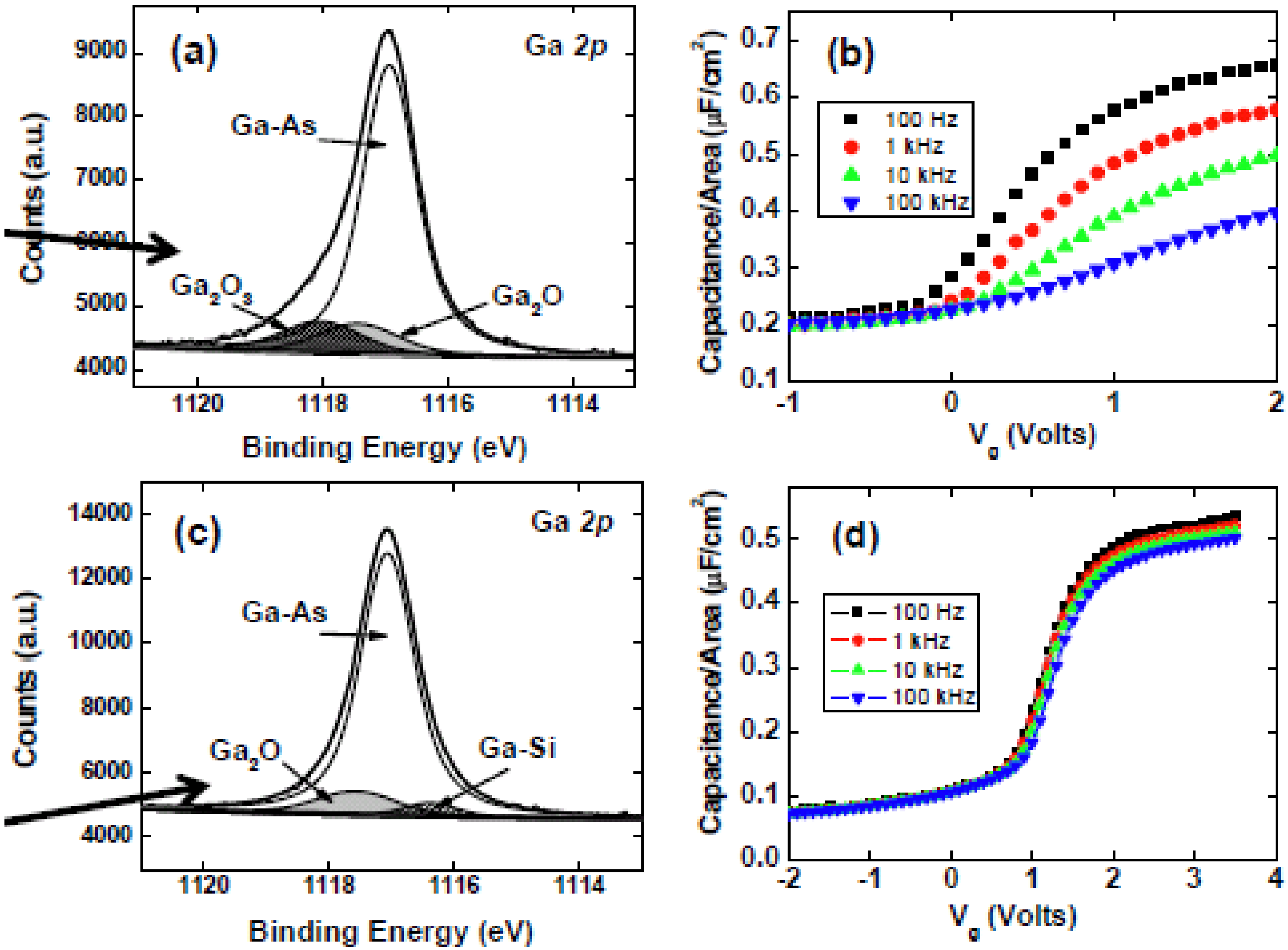
1. Pt is used to eliminate traps at metal/TiO_2.
2. More trap features appear across the spectrum.
3. Attributable to GaAs interface traps

interface traps in upper half of GaAs band gap

XPS Study Indicates Crucial Effect of Ga_2O_3

XPS Data *vs* C-V Data: Ga_2O_3 Degrades Interface Quality

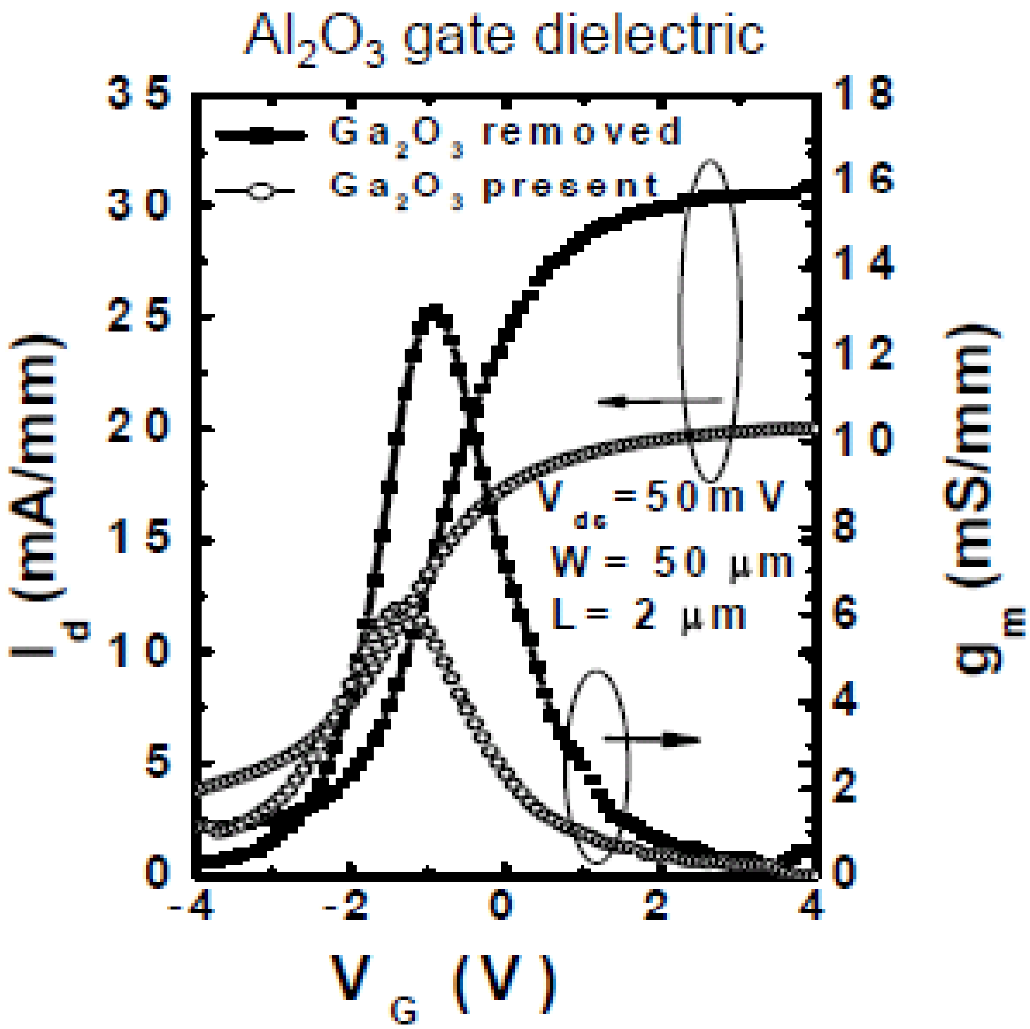
Hinkle et al., APL **94**, 162101 (2009)



With Ga_2O_3

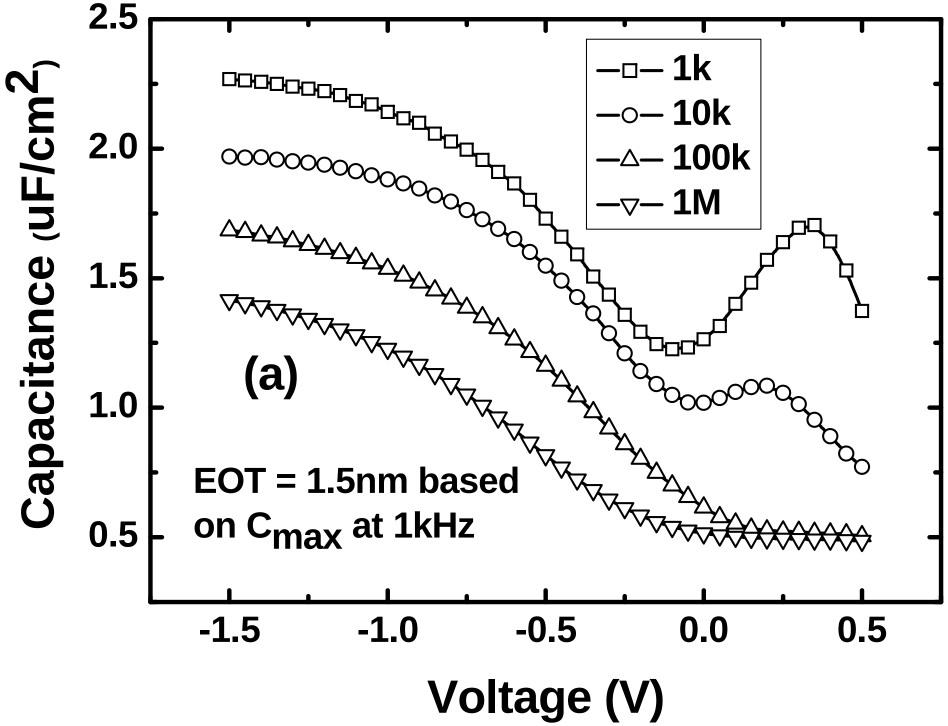
Without Ga_2O_3

I_d and G_m Improve with Ga_2O_3 Removed

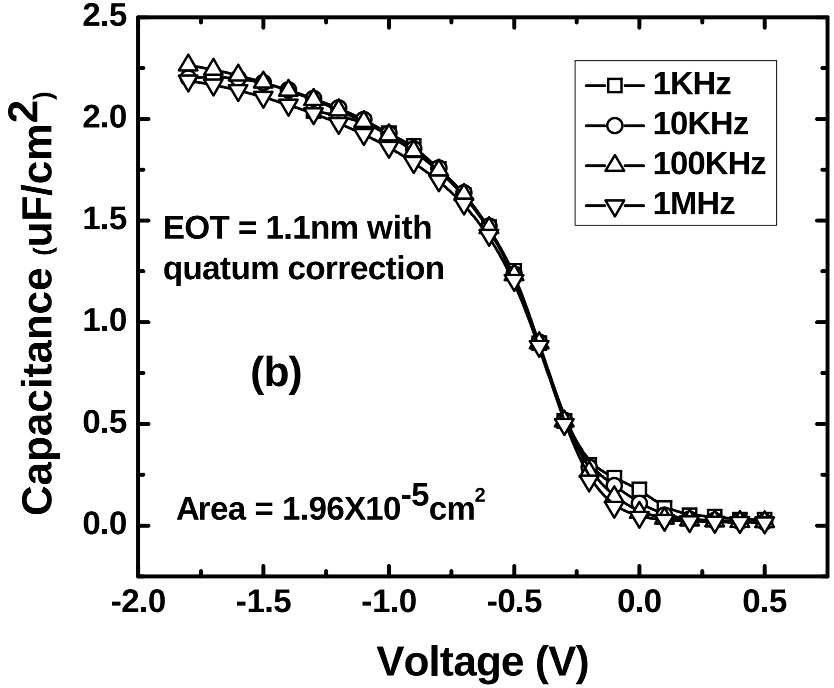


$In_{0.53}Ga_{0.47}As$ MOS C-V characteristics

TiO_2-Al_2O_3/$In_{0.53}Ga_{0.47}As$



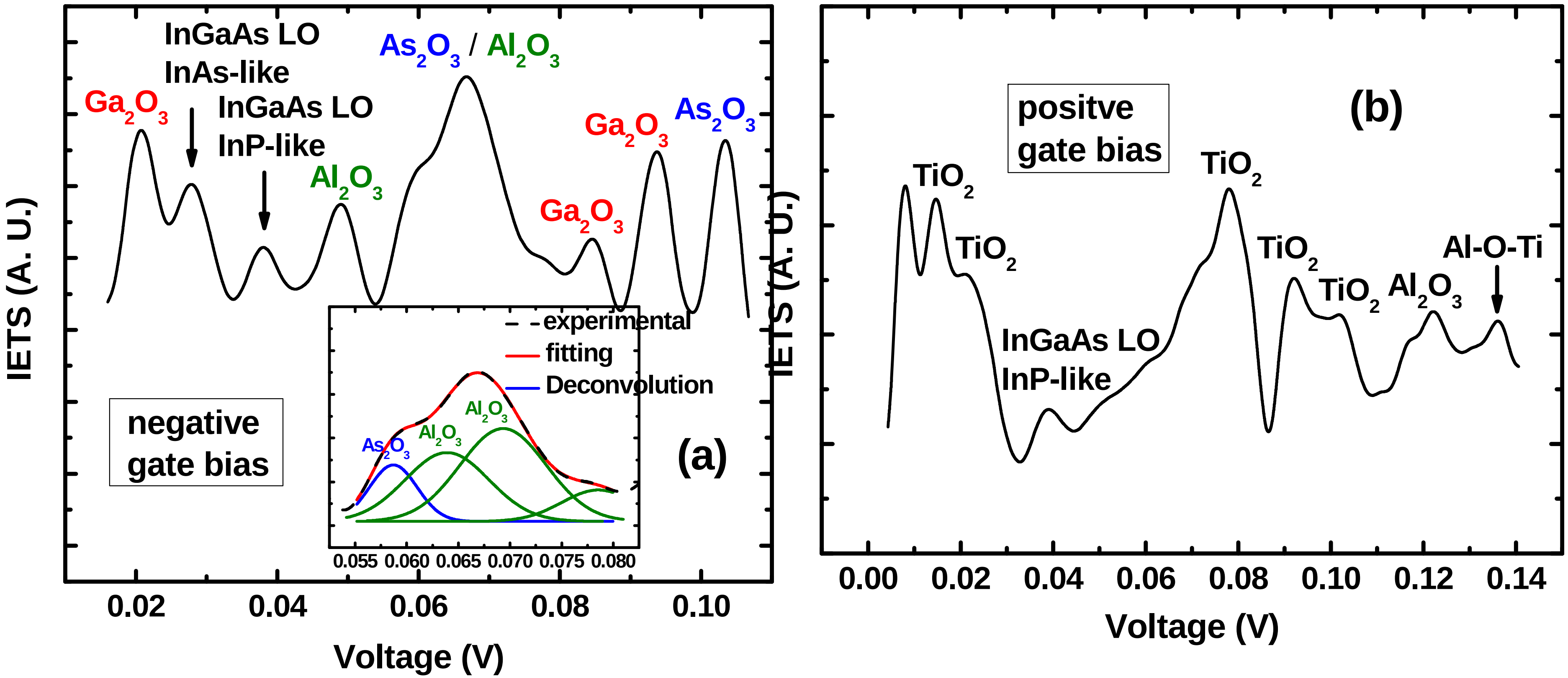
Si control sample



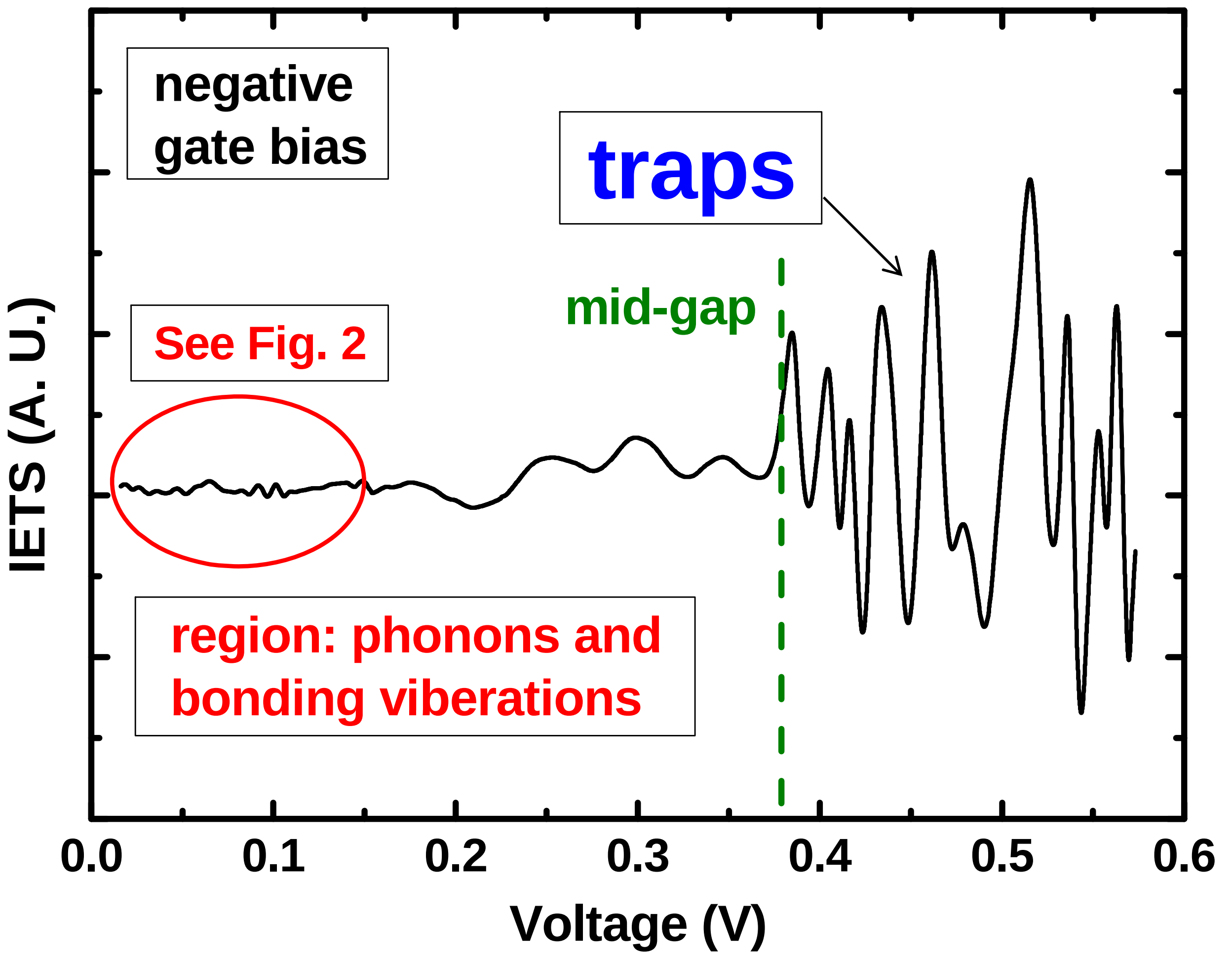
IETS spectra of $In_{0.53}Ga_{0.47}As$ MOS

Gate negatively biased

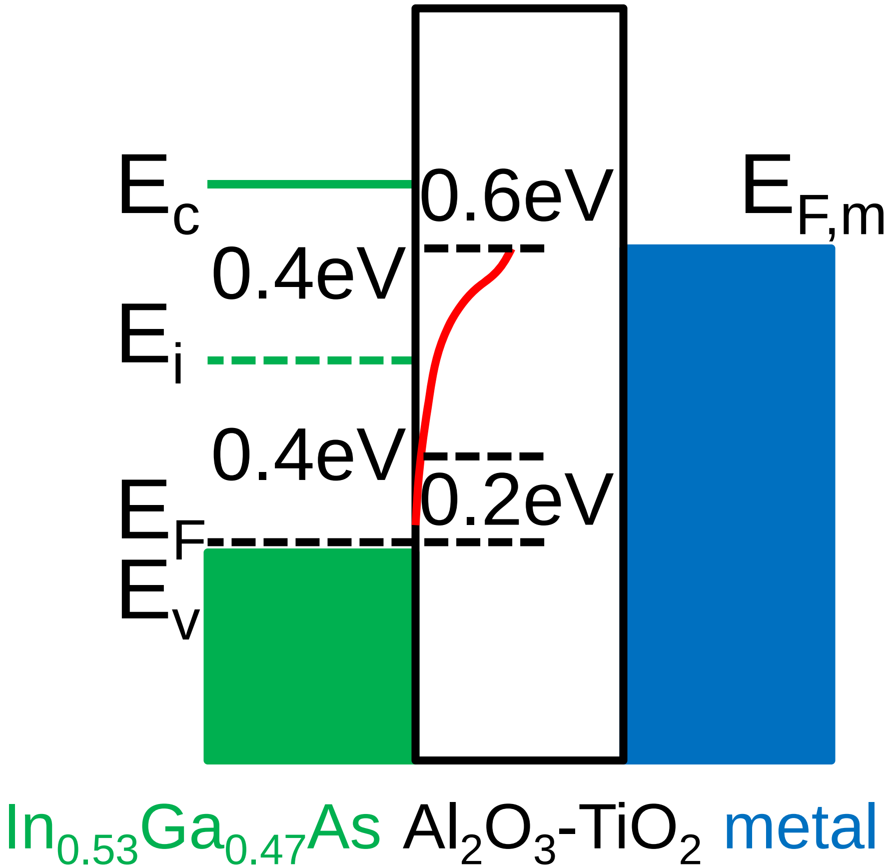
Gate positively biased



Huge trap features in $In_{0.53}Ga_{0.47}As$ MOS

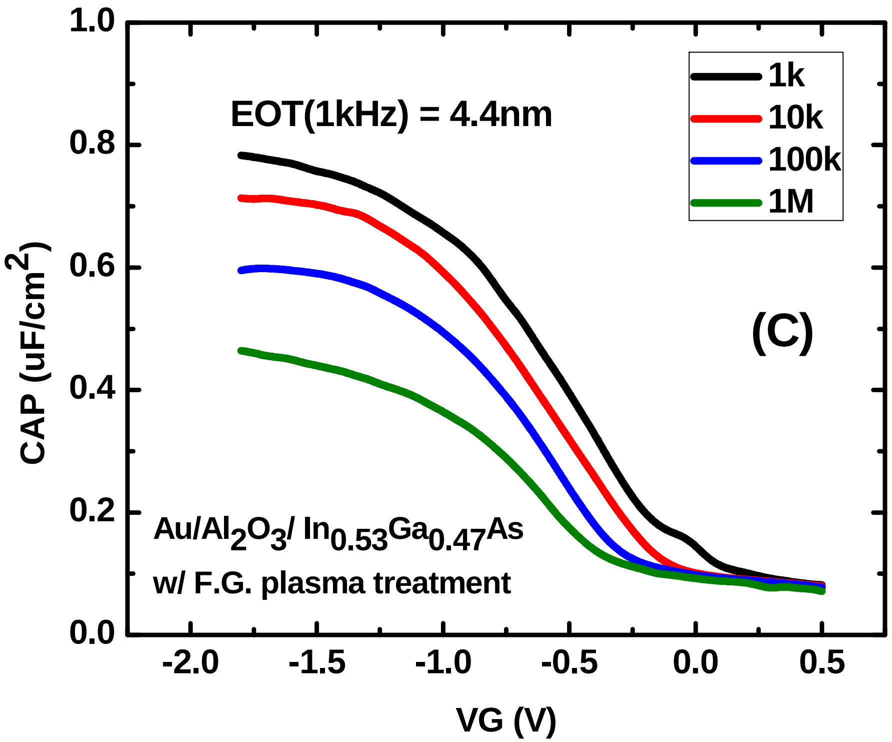


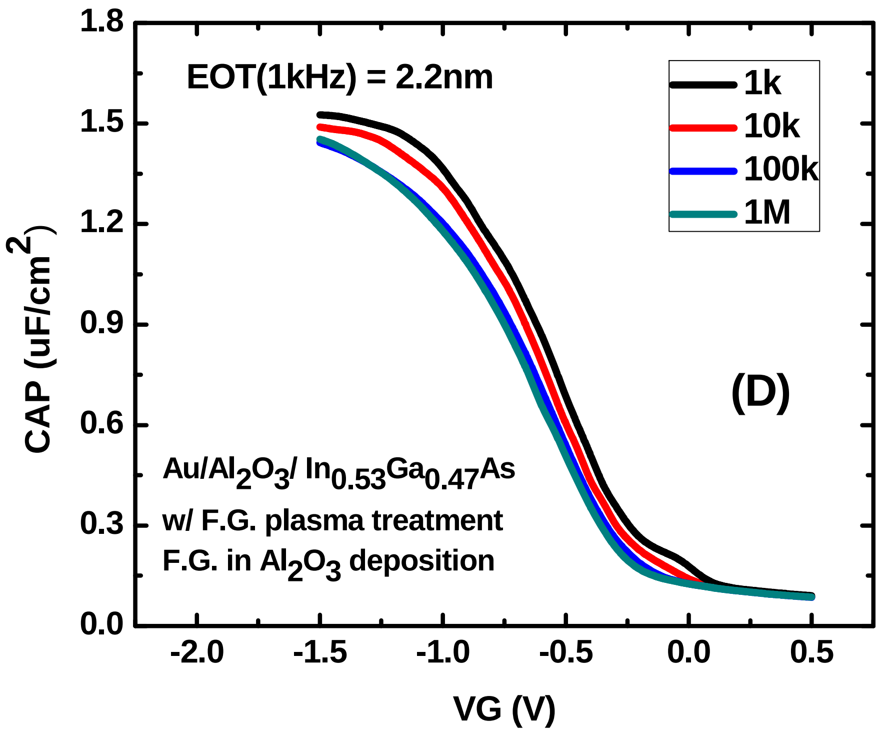
Trap location/energy analysis



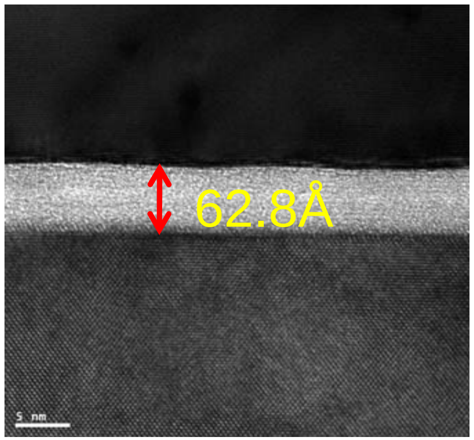
- Interface traps start to appear at ~0.2eV above E_F(VG=0)~E_v of p-type $In_{0.53}Ga_{0.47}As$
- Density of interface traps greatly increases above mid-gap.

Effect of H_2 During Al_2O_3 Deposition

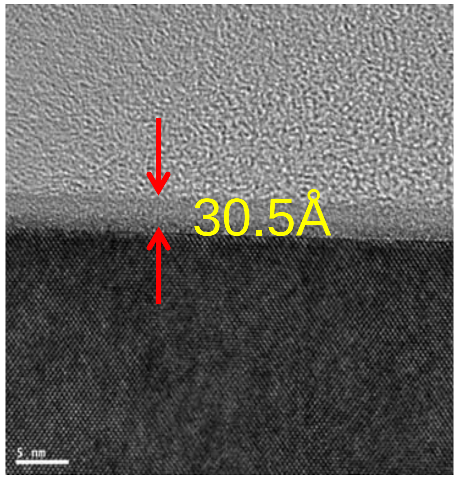




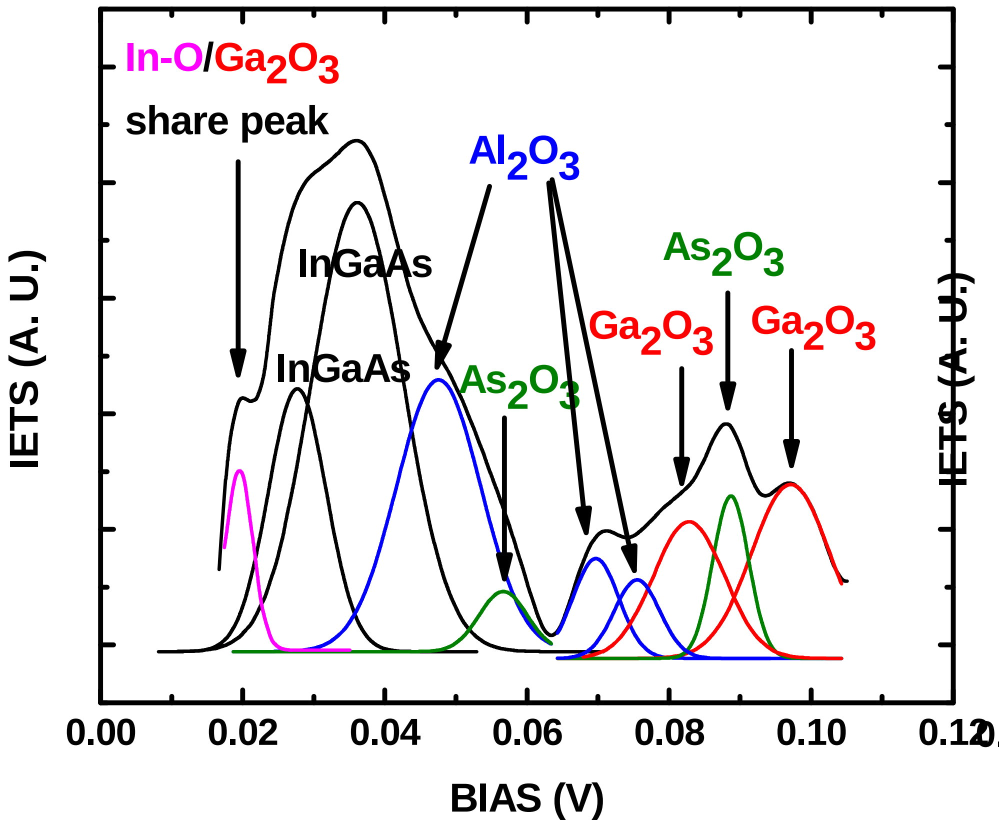
Without H_2



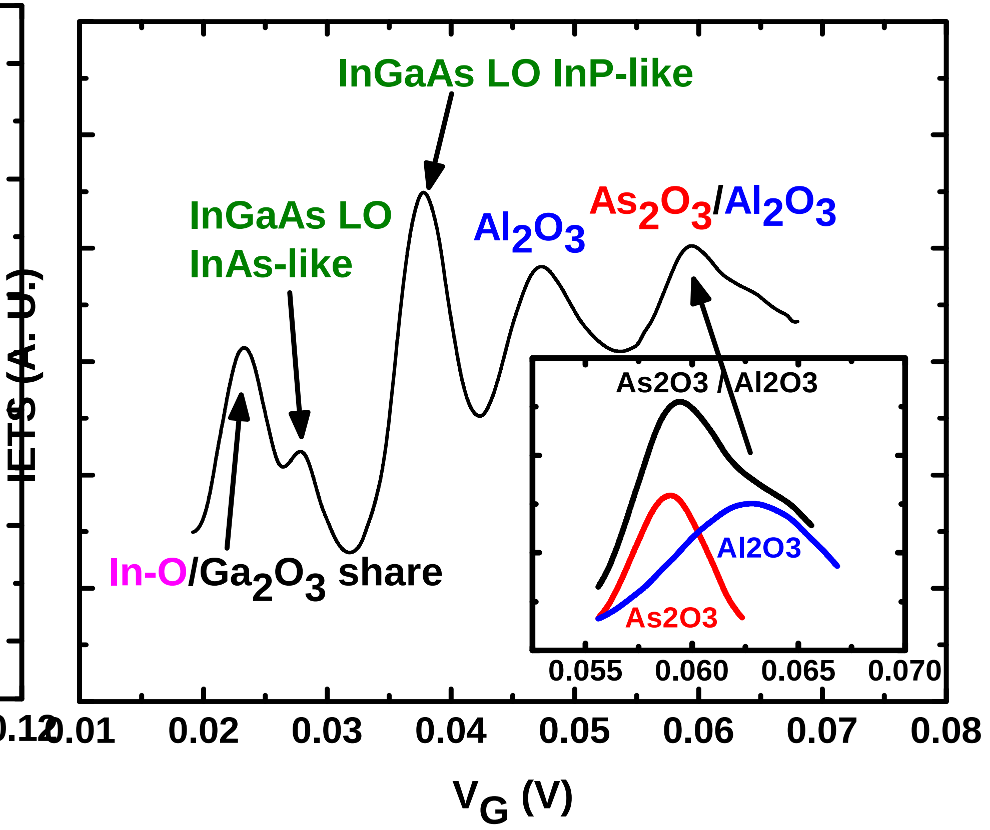
With H_2



Effect of H_2 During Al_2O_3 Deposition



Without H_2



With H_2

Major difference is Ga_2O_3

Summary

- IETS reveals phonons, bonding vibrations, and defects in ultra-thin gate stacks.
- IETS probes preferentially near the positive electrode.
- Traps in gate stack exhibit distinct IETS signatures.
- Trap energy and its physical location can be determined from forward and reverse-biased IETS spectrum.
- IETS can be a valuable tool for studying new gate stacks such as those on InGaAs.