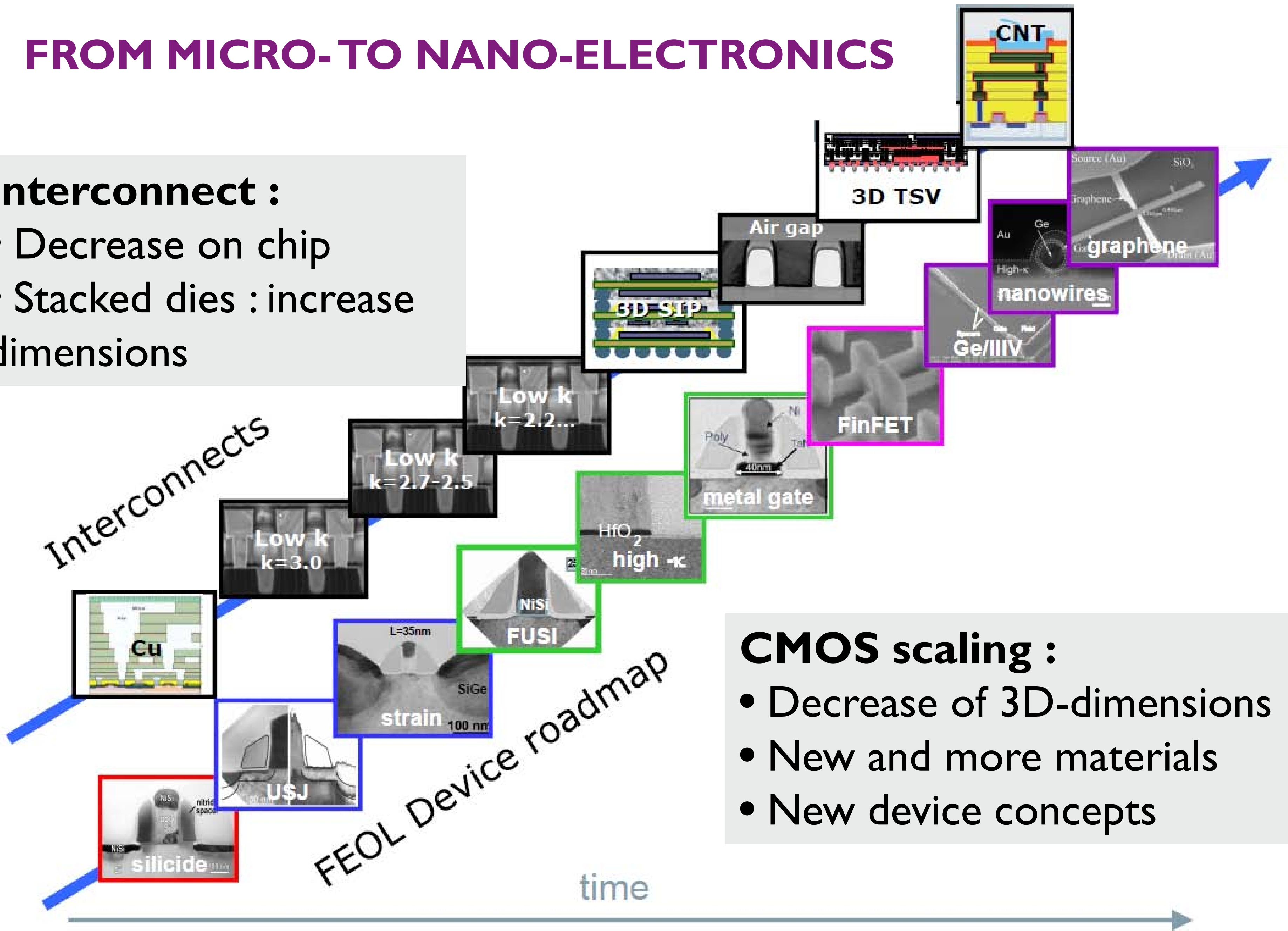
W.Vandervorst


FROM MICRO- TO NANO-ELECTRONICS
Interconnect :
• Decrease on chip
• Stacked dies : increase dimensions
Interconnects
Cu
Low k
k=3.0
Low k
k=2.7-2.5
Low k
k=2.2…
3D SIP
Air gap
3D TSV
CNT
FEOL Device roadmap
silicide
USJ
L=35nm
SiGe
strain
100 nm
NiSi
FUSI
HfO2
high -κ
Poly
metal gate
FinFET
Ge/IIIV
Au
Ge
High-κ
nanowires
Source (Au)
SiO2
graphene
CMOS scaling :
• Decrease of 3D-dimensions
• New and more materials
• New device concepts
time

IMPLICATIONS OF SCALING ON METROLOGY : MATURE AND EMERGING SOLUTIONS

(S)TEM-Tomography,

C-AFM, SSRM, Atomprobe

TEM-tomography

Atomprobe

3D-SSRM

analysis

EXLE-SIMS, Zero-energy SIMS, AR-XPS

Analytical (S)TEM, C-AFM

SSRM

TEM (NBD, M-EH)

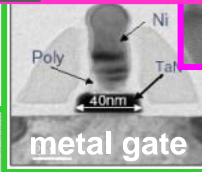
USJ

strain

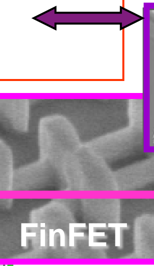
SiGe

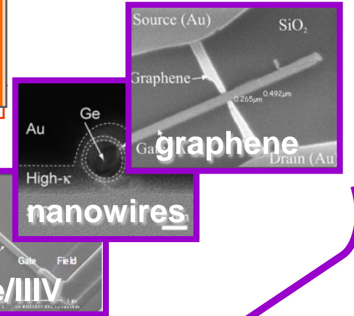
FUSI

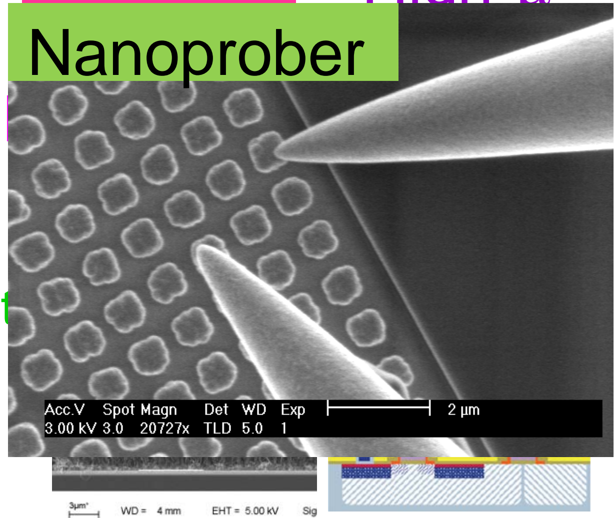
high -κ



FinFET







>=130

90-65-45

Strain, USJ

45-32

High-κ, Metal Gat

16 and beyo

High-µ

time

What’s New at Imec (for you)

Metrology

PMOR		**We-28**			
EXLE-Sims					
SSRM					
C-AFM					
XPS					
Atomprobe					
EDX				Th-20	
TEM				TU-28	TU-11/Th-10
		Activation carriers	**Dopants diffusion**	**Layer growth interactions**	**3D-(finfet) Confined volume**

Materials and process development

© IMEC 2010

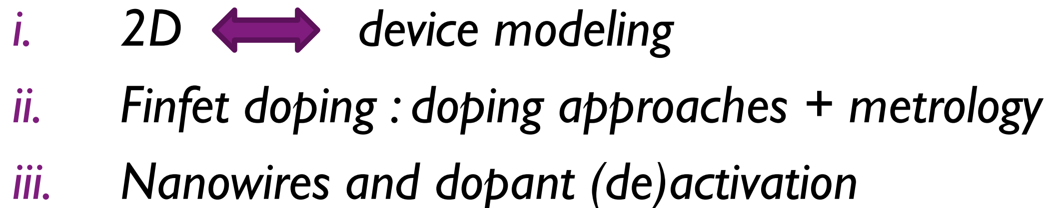
OUTLINE

1. Enhanced Metrology : PMOR

   From I/I SPC to non-contact carrier profiling in 10 micron area.

2. Material/process fundamental understanding through enhanced metrology

   A. Dopants/carriers

      i. *2D*  *device modeling*

      ii. *Finfet doping : doping approaches + metrology*

      iii. *Nanowires and dopant (de)activation*

   B. Layer growth/material interactions

      i. *Passivating Ge with Si : EXLE-SIMS*

      ii. *AP of high k : image # reality (cfr M.Brillouet)*

      iii. *Metal gate high k interaction : BS C-AFM/XPS*

      iv. *ReRam*

      v. *Looking for empty space*

      vi. *Quantitative phase analysis*

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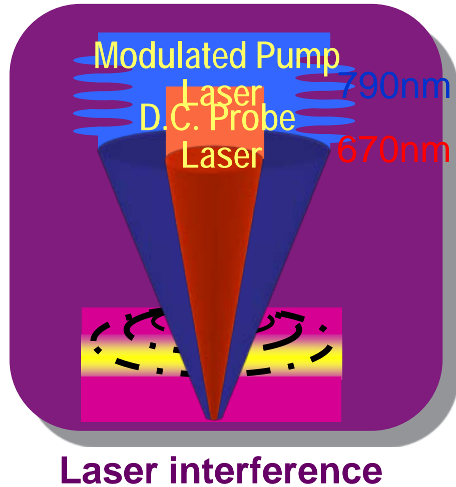
SPC *Before Anneal :The conventional application*

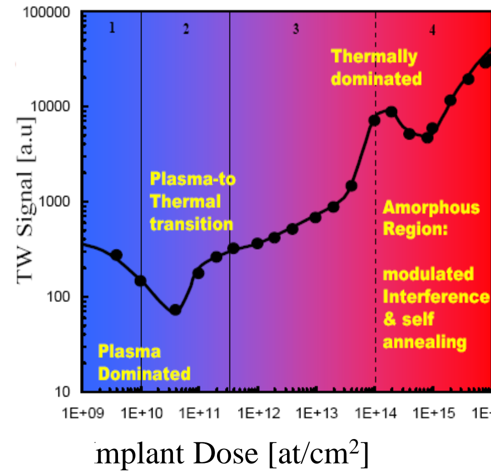
In-line USJ Metrology With Photomodulated Reflectance

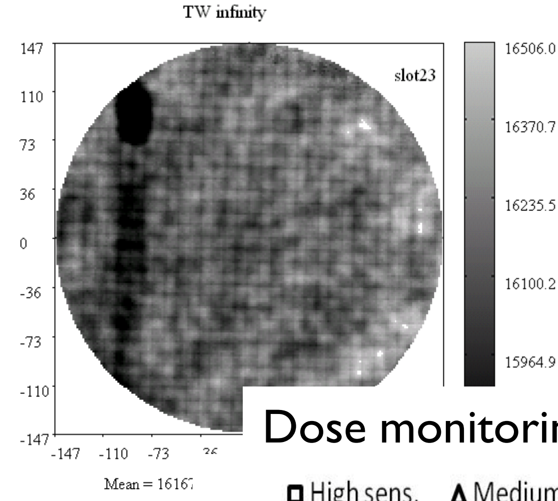
PMOR with Therma-Probe® (TP):

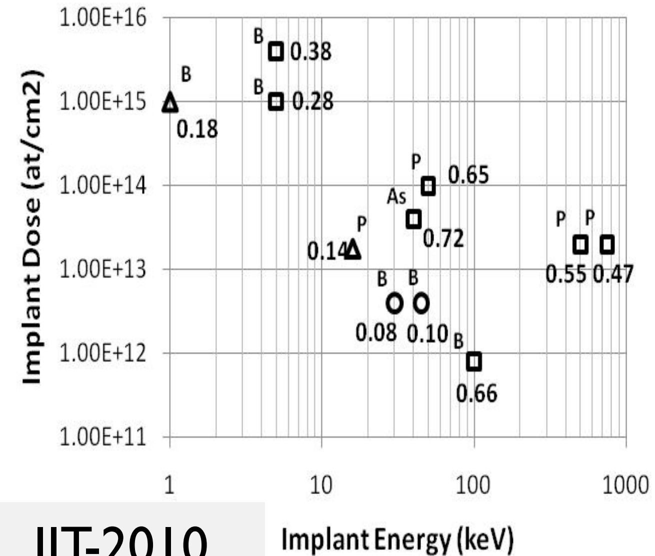
dose monitoring (as-implanted)

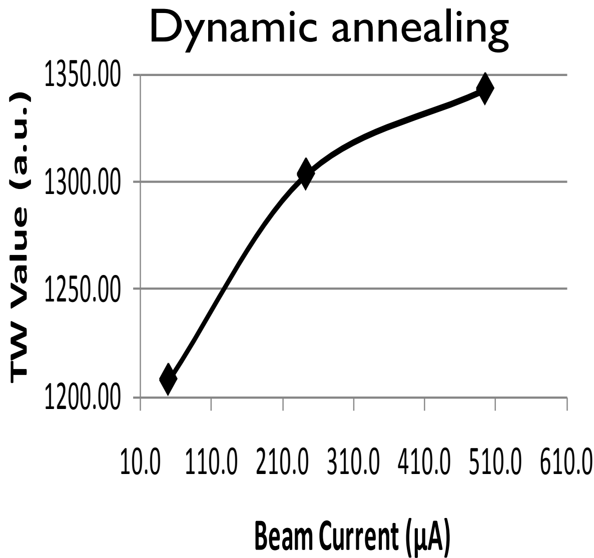


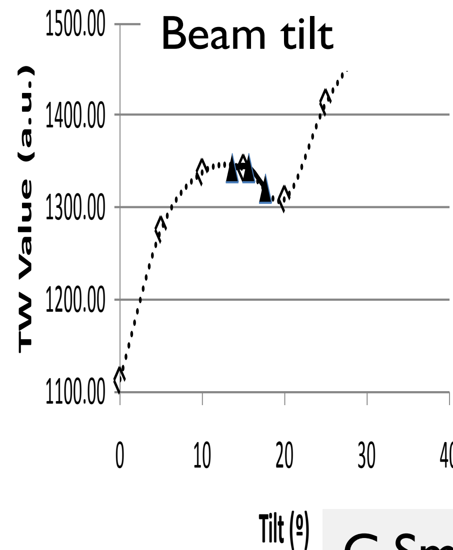
Laser interference





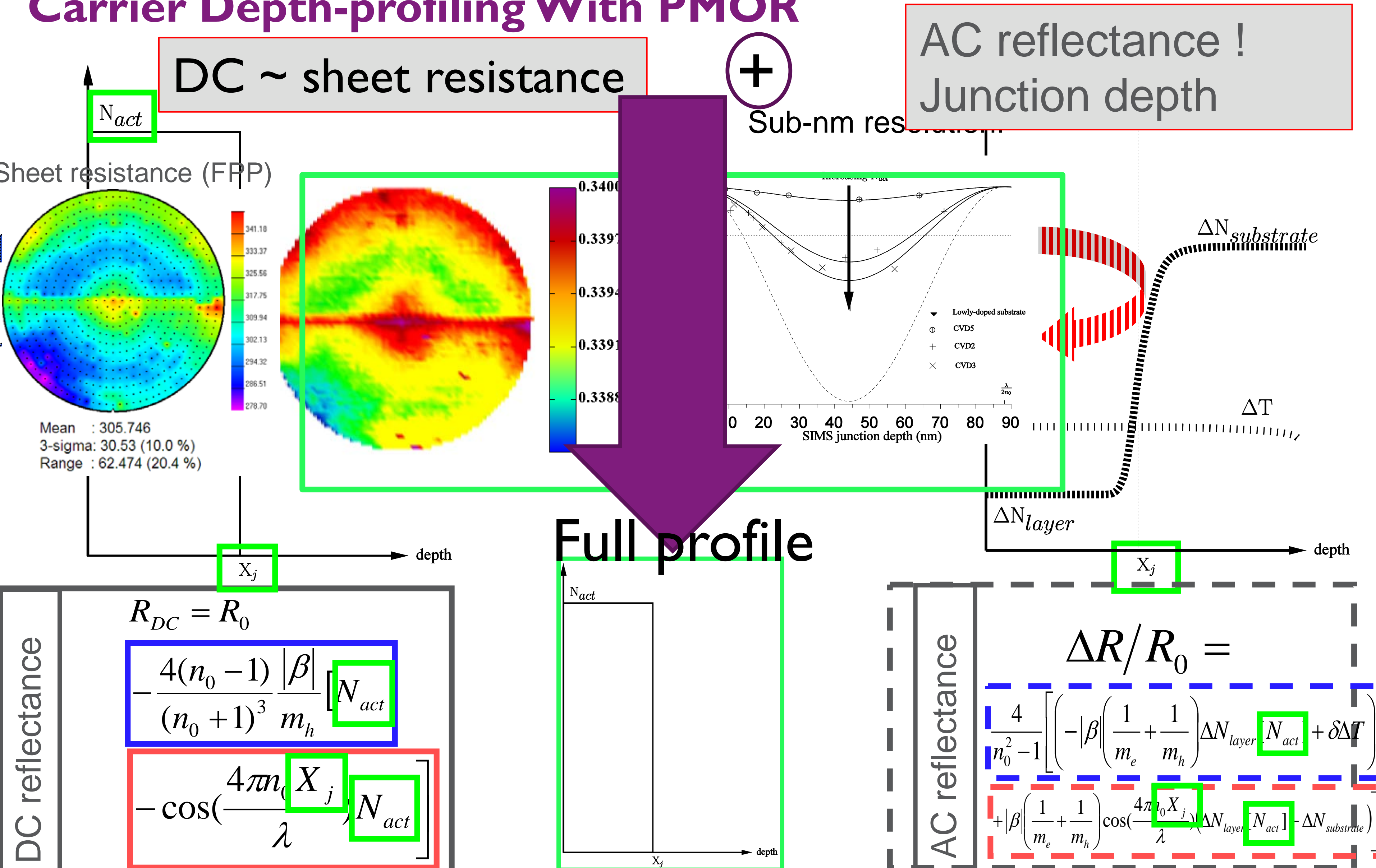






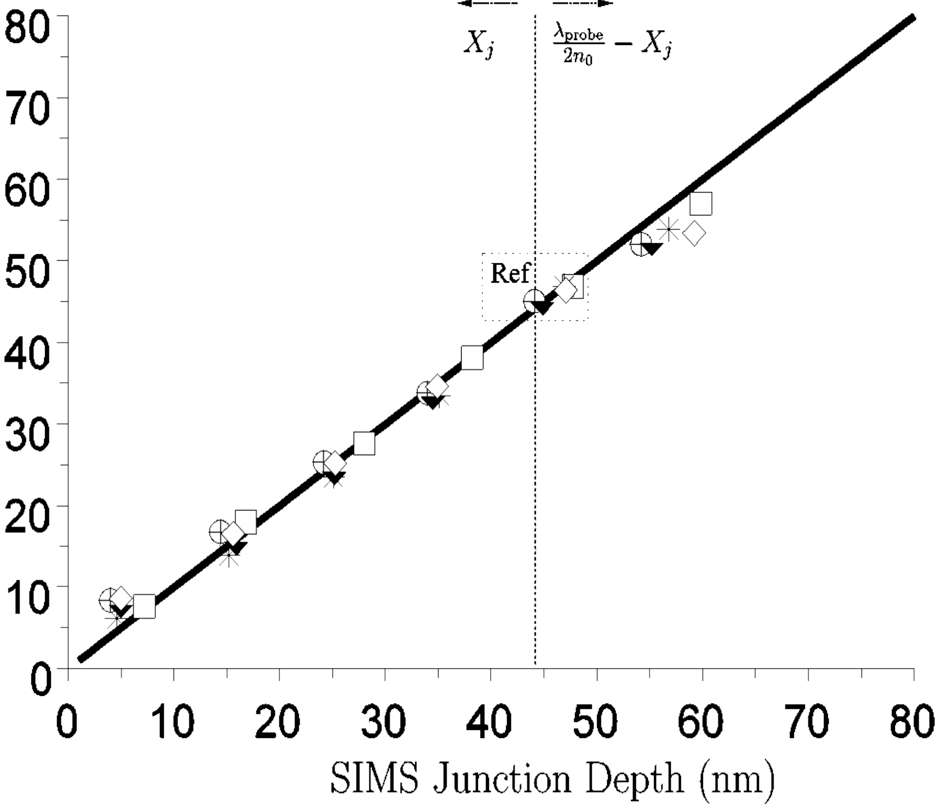
G.Smets et al., IIT-2010

The new approach : SPC AFTER anneal
Carrier Depth-profiling With PMOR



*J. Bogdanowicz et al., *Electrothermal Theory of Photomodulated Optical Reflectance on Active Doping Profiles in Silicon*, JOURNAL OF APPLIED PHYSICS **108, 104908 (2010)** , **25 pp!!**

Non-destructive, Non-contact Extraction Of Junction Depths



TP @ 3μm separation

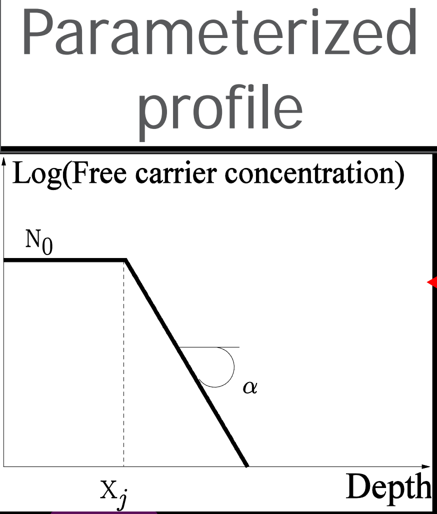
JPV technique

•J. Bogdanowicz et al., *Nondestructive Extraction of Junction Depths of Active Doping Profiles from Photomodulated Optical Reflectance Offset Curves, JVST B, 28, 227 (2010)*

Carrier Profiling With PMOR :
Solving The INVERSE Problem through fundamental understanding

Fundamental Model of PMOR(*)

Parameterized profile



•Transport Model

From ***profile*** to ***plasma and thermal*** waves:

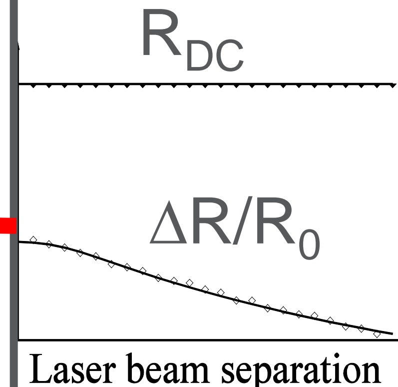
$$\begin{cases} -\vec{\nabla}.\varepsilon\vec{\nabla}V = q(P-N+C(z)) \\ i\omega\Delta N = 1/q\vec{\nabla}.\vec{J}_n + G - R \\ i\omega\Delta P = -1/q\vec{\nabla}.\vec{J}_p + G - R \\ i\rho c_p\omega\Delta T = k_{th}\vec{\nabla}.\vec{\nabla}T + G_{th} \end{cases}$$

•Optical Model

From ***profile and waves*** to ***signals***:

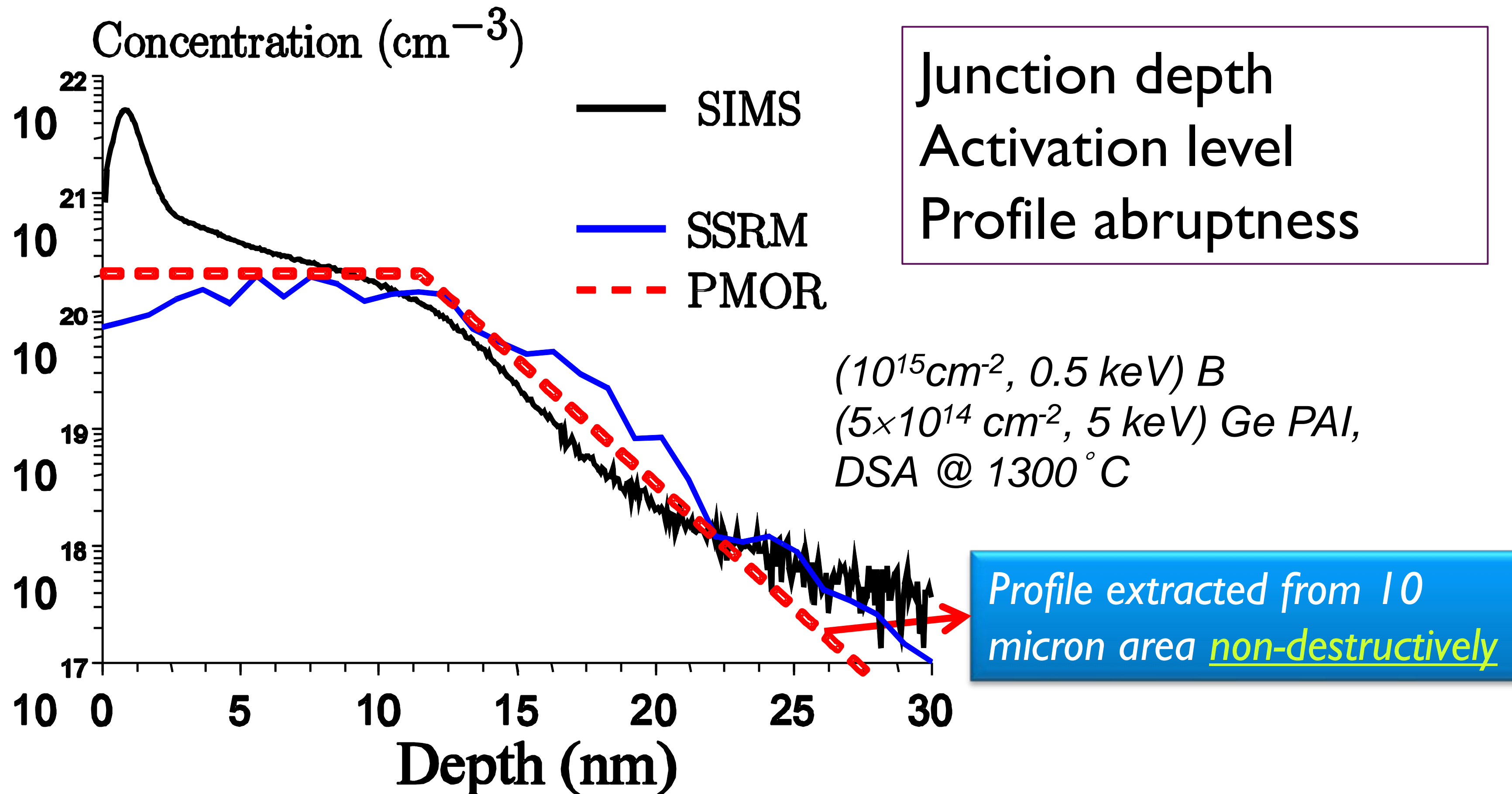
$$R_{DC} = R_0 - \frac{4(n_0-1)}{(n_0+1)^3}\frac{|\beta|}{m_h}\left[N_{act}(z=0) + \int_{0+}^{+\infty}\frac{\partial N_{act}(z)}{\partial z}\cos\left(\frac{4\pi n_0 z}{\lambda_{probe}}\right)dz\right]$$

$$\Delta R/R_0 = \frac{4}{n_0^2-1}\left[\left(-|\beta|\left(\frac{1}{m_e}+\frac{1}{m_h}\right)\Delta N(z=0) + \delta\Delta T\right) - |\beta|\left(\frac{1}{m_e}+\frac{1}{m_h}\right)\int_{0+}^{+\infty}\frac{\partial \Delta N(z)}{\partial z}\cos\left(\frac{4\pi n_0 z}{\lambda_{probe}}\right)dz\right]$$



*J. Bogdanowicz et al., *Electrothermal Theory of Photomodulated Optical Reflectance on Active Doping Profiles in Silicon,* accepted for publication in Journal of Applied Physics (2010),

Non-contact Reconstruction Of Annealed Implanted Profiles



•J. Bogdanowicz et al., *Non-Destructive Characterization of Activated Ion-Implanted Doping Profiles Based on Photomodulated Optical Reflectance,*
•AIP Proceedings Series, Proceedings of 2010 IIT conference (Kyoto)

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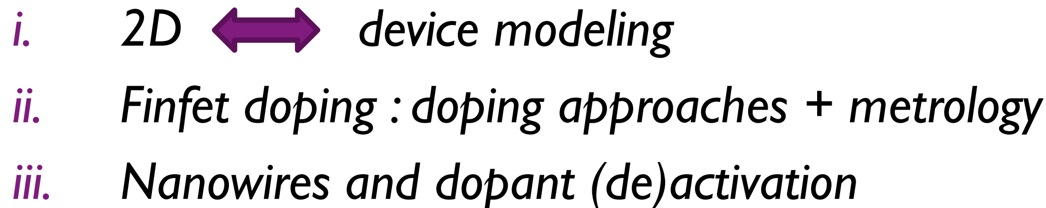
2. Material/process fundamental understanding through enhanced metrology

   A. Dopants/carriers



   i. *2D ⟺ device modeling*

   ii. *Finfet doping : doping approaches + metrology*

   iii. *Nanowires and dopant (de)activation*

   B. Layer growth/material interactions

   i. *Passivating Ge with Si : EXLE-SIMS*

   ii. *AP of high k : image # reality (cfr M.Brillouet)*

   iii. *Metal gate high k interaction : BS C-AFM/XPS*

   iv. *ReRam*

   v. *Looking for empty space*

   vi. *Quantitative phase analysis*

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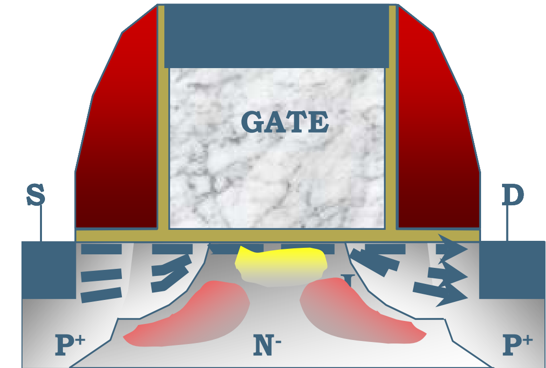
Doping and Metrology Challenges

1. Planar (CMOS)-devices

   1D-profiles are no more relevant,

   need for 2D-doping &

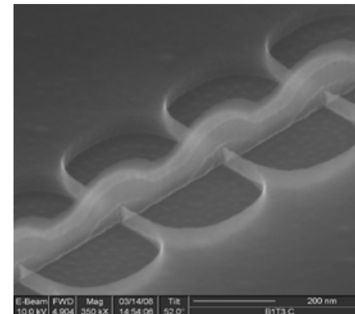
   2D-profiling with sub-nm resolution

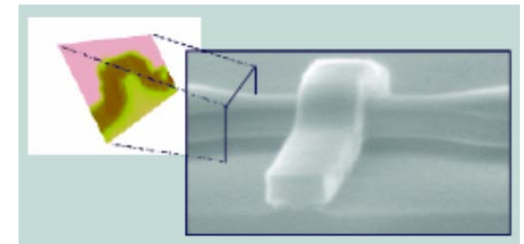


2. 3D-devices : FINFET

   Need for conformal doping

   Need for 3D-resolution

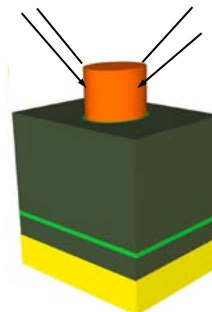


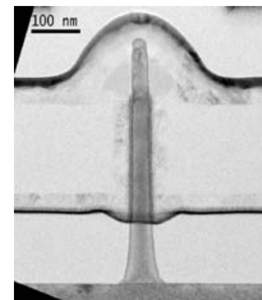


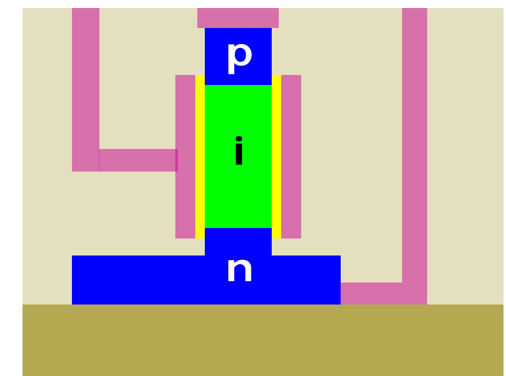
3. Confined volume : NW-FET (TFET)

   3D-doping

   localized analysis

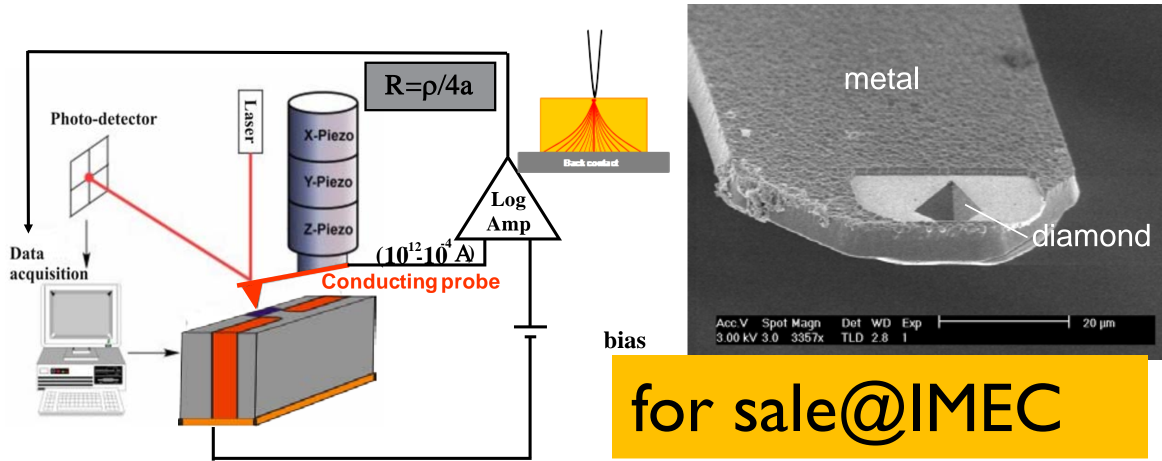




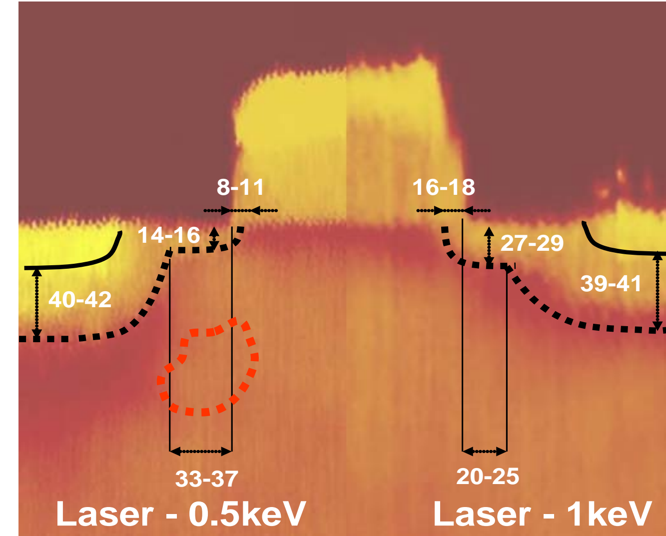


SSRM Carrier Profile Metrology : A Mature Asset In Technology Development

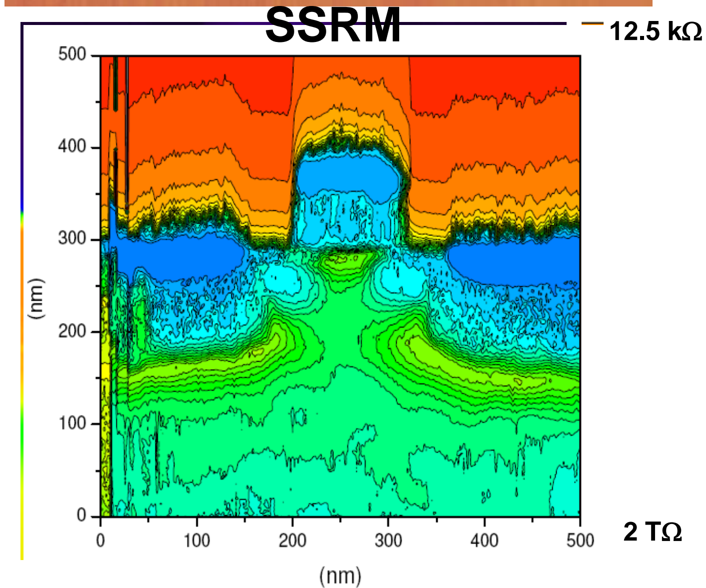
Junction engineering



for sale@IMEC



	ITRS 2005	ITRS 2010	SSRM	ITRS 2016
Lateral/vertical steepness (nm/dec)		+	1-1.5	
Lateral/depth resolution (nm)		+	0.5 - 1	
Concentration precision (%)		+	3-5%	
Dynamic range (at/cm3)			10^{15} - 10^{21}	



P.Eyben, W.Vandervorst, D.Alvarez,, M.Xu. and M.Fouchier, in "Scanning Probe Microscopy, Electrical and Electromechanical Phenomena at the Nanoscale"*, edited by S. Kalinin and A. Gruverman (Springer, New York, 2007), Vol. 1, Chapter 2, '"Scanning spreading resistance microscopy"*

imec © IMEC 2010

How to Exploit SSRM Profiles for Process AND Device Optimization?

- **APPROACH I :**
  - **Step 1 : Calibrate process simulations to match SSRM-profiles**

- *Accuracy models for Non-equilibrium processes (msec, plasma doping,..)*

+ *Framework for TCAD based process optimization*

  - **Step 2 : Use TCAD profiles as input towards device simulation**
  - ?? Perfect match TCAD --- SSRM
  - ?? Slow
- **Approach II** : Use SSRM profile as input to device simulator
  - Import syntax
  - Identify structure (gate, oxide, silicides,…)
  - Required accuracy, sensitivity

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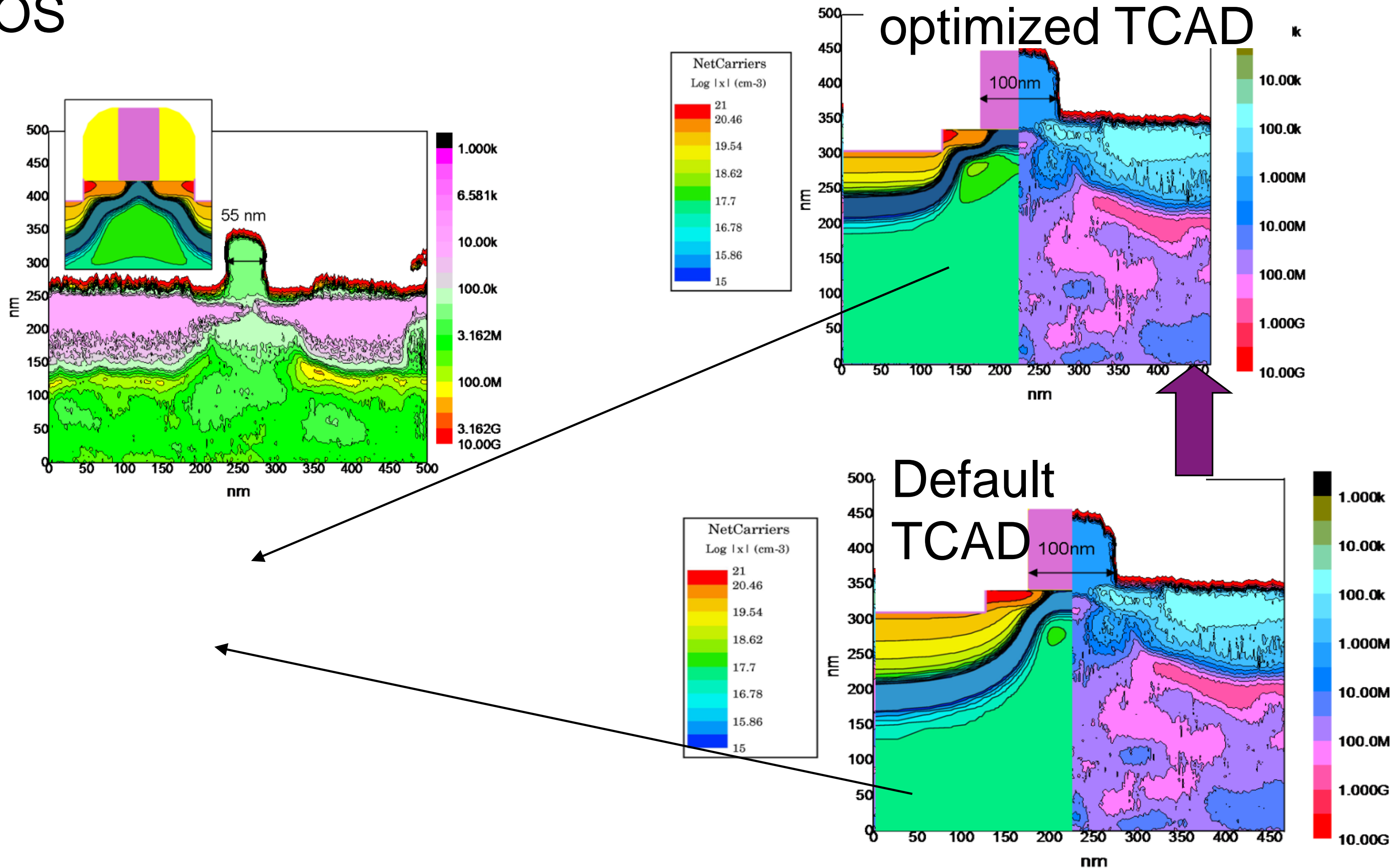
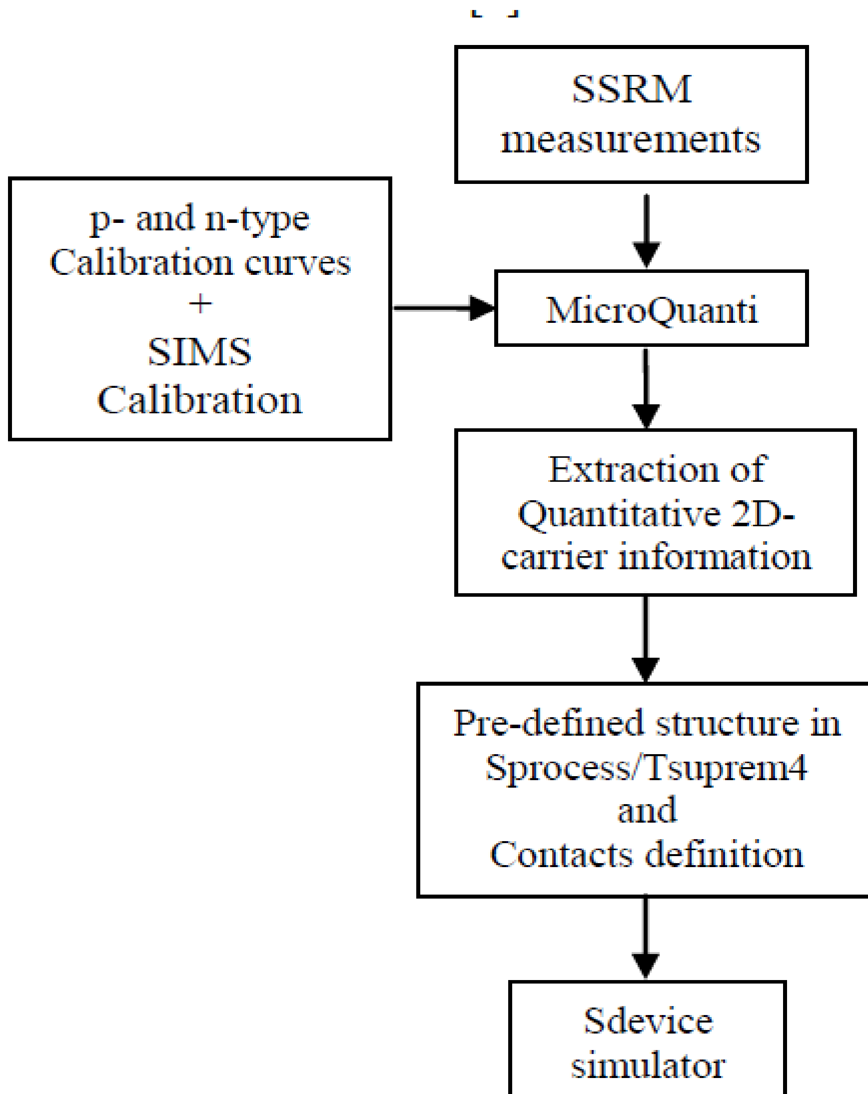
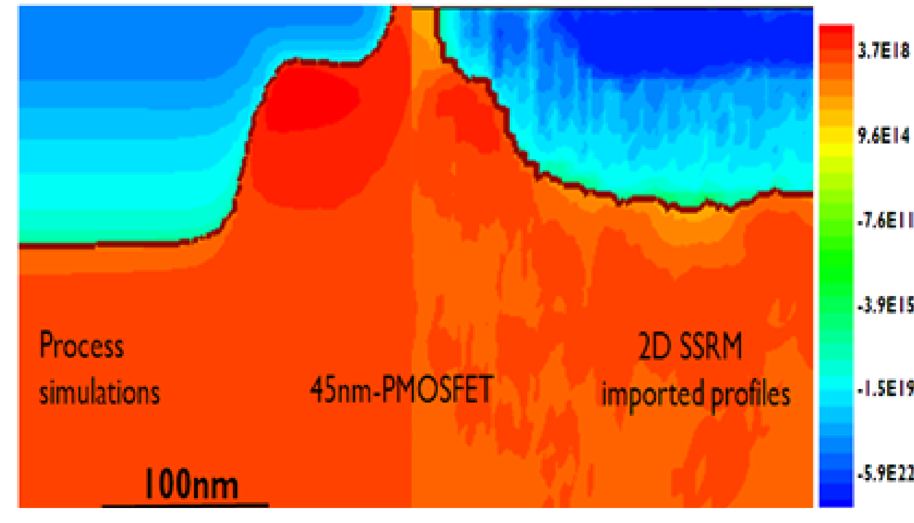
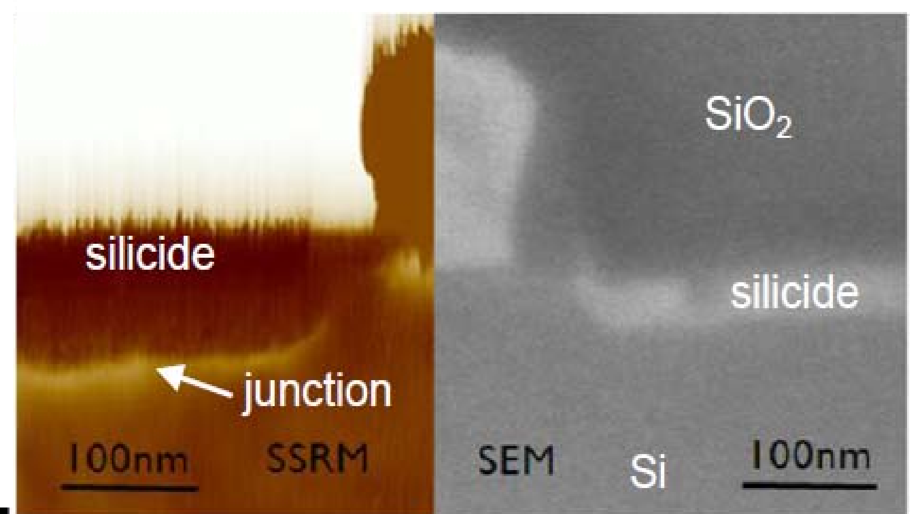
(HV) SSRM as a Tool for TCAD Calibration



Predicting Device Performance with SSRM Distributions







A.Nazir et al., to be published

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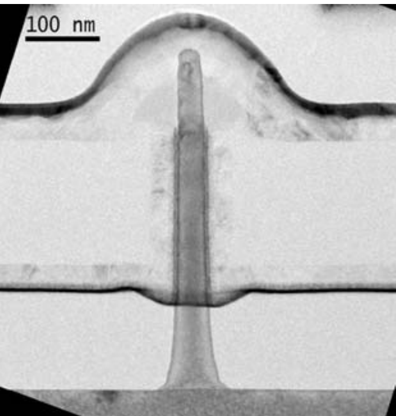
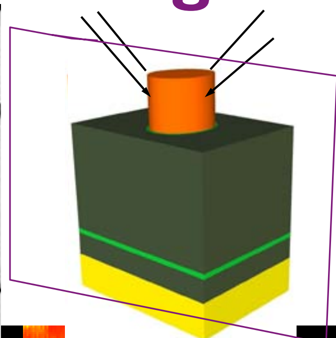
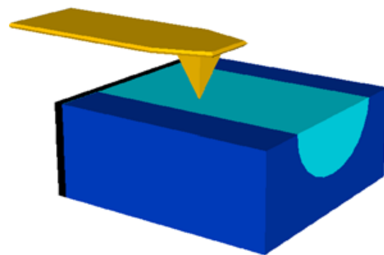
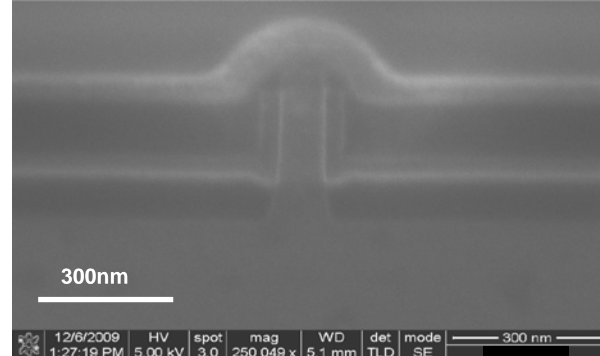
Carrier Profiling In Si NW-TFET









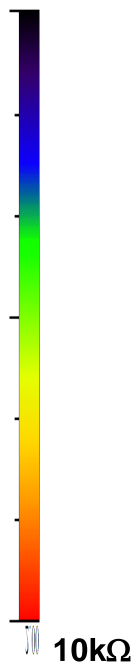
Boron implant

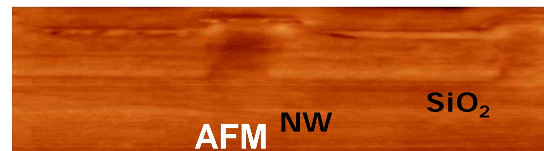
Cap layer

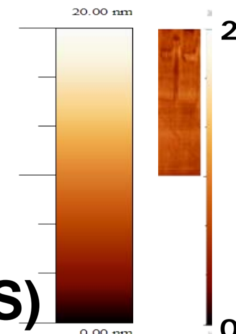
Metal-gate

Dopant Diffusion

100nm



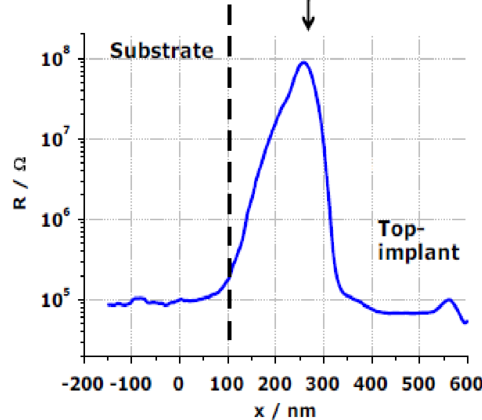


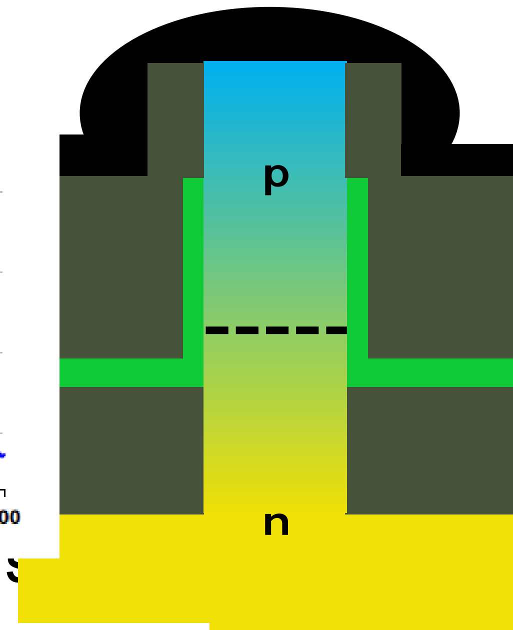


Substrate

400nm

0.8 nm (RMS)

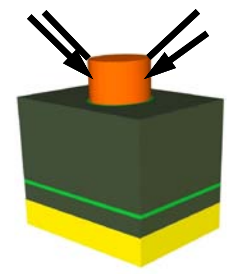


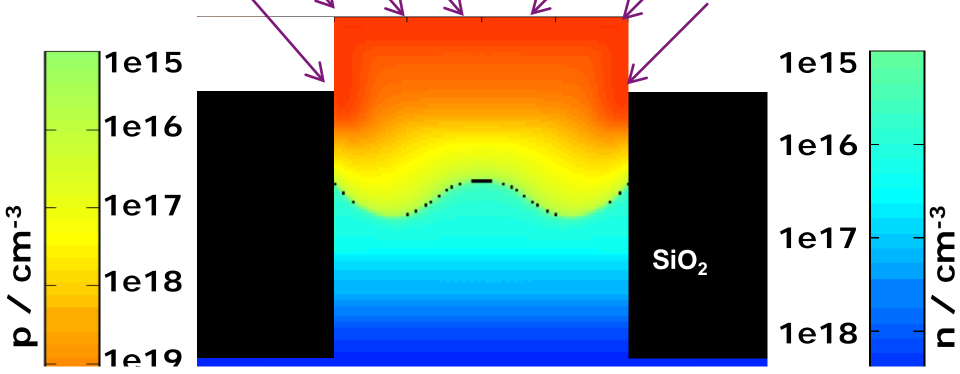


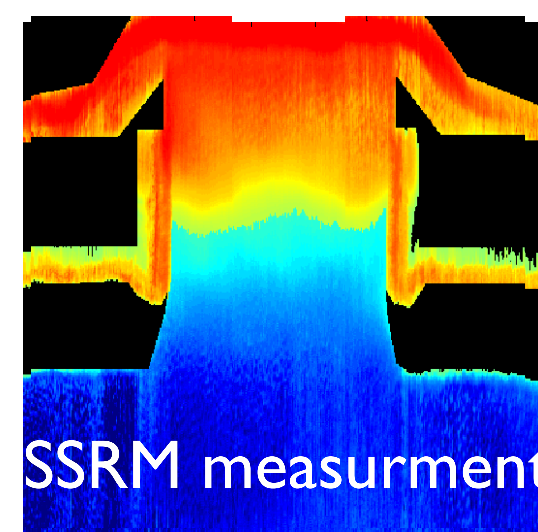
SSRM result

A,Schulze et al. Nanotechnology 22 (2011) 185701.

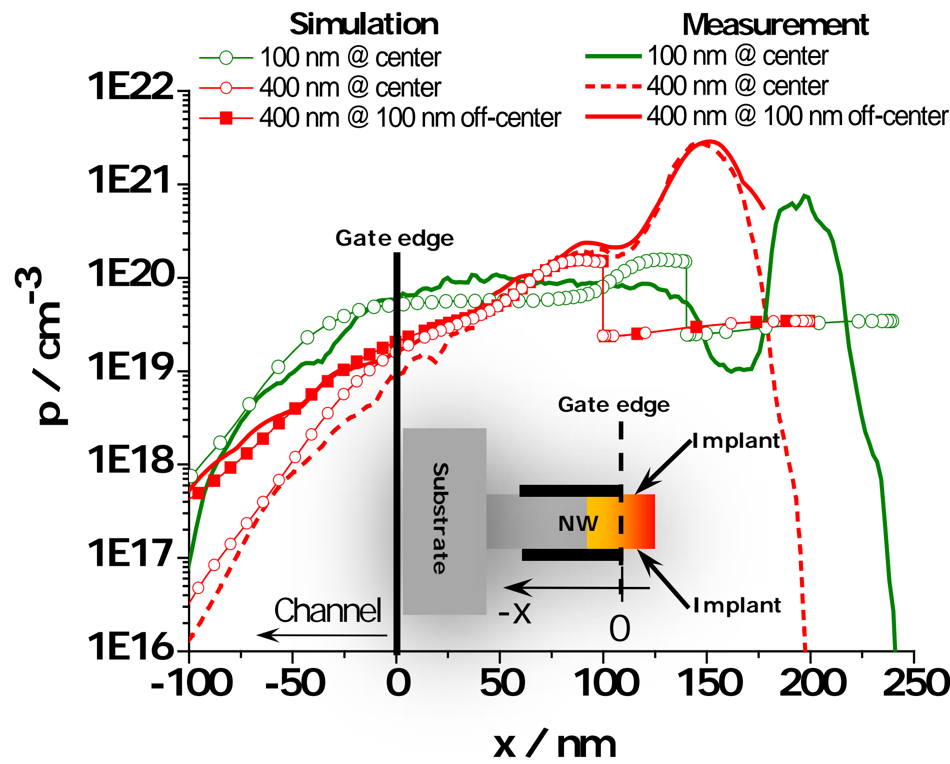
Size Dependent Carrier Distributions

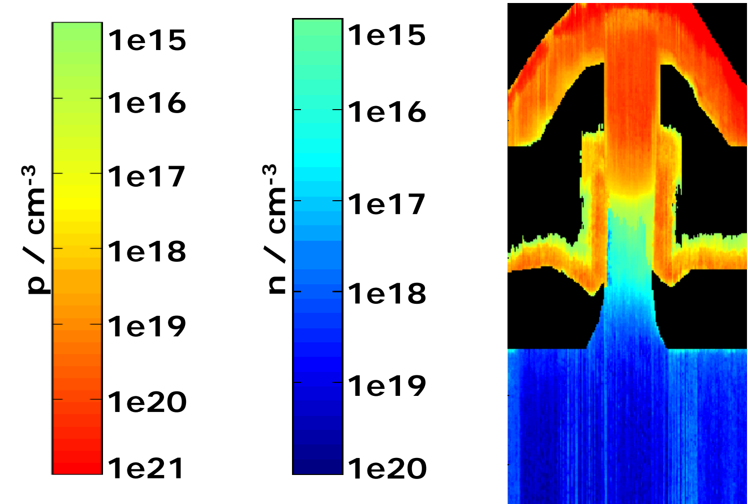






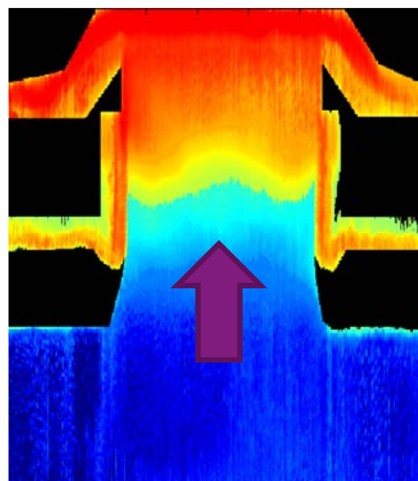
NW ∅ 400 nm

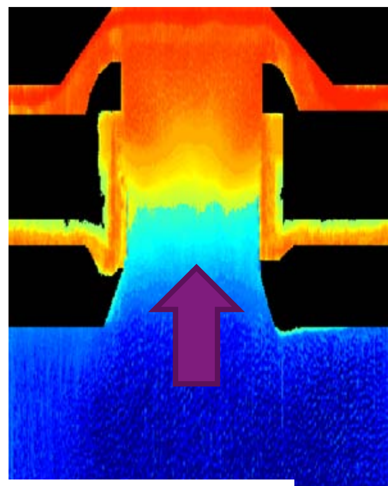


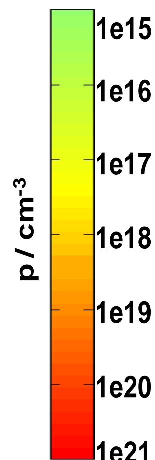


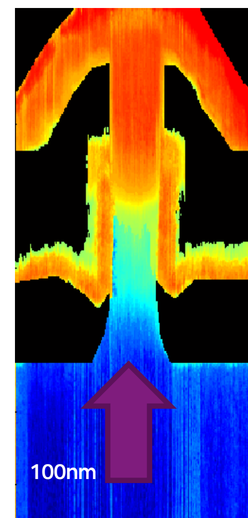
NW ∅ 100 nm

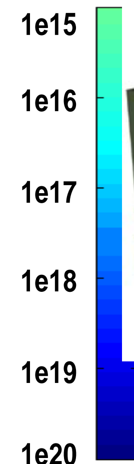
(Unexpected) size dependent deactivation in n-region

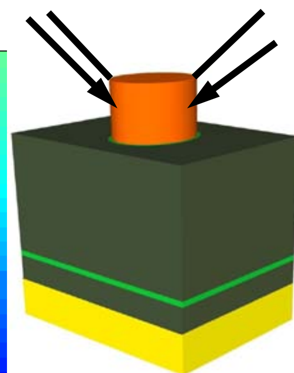


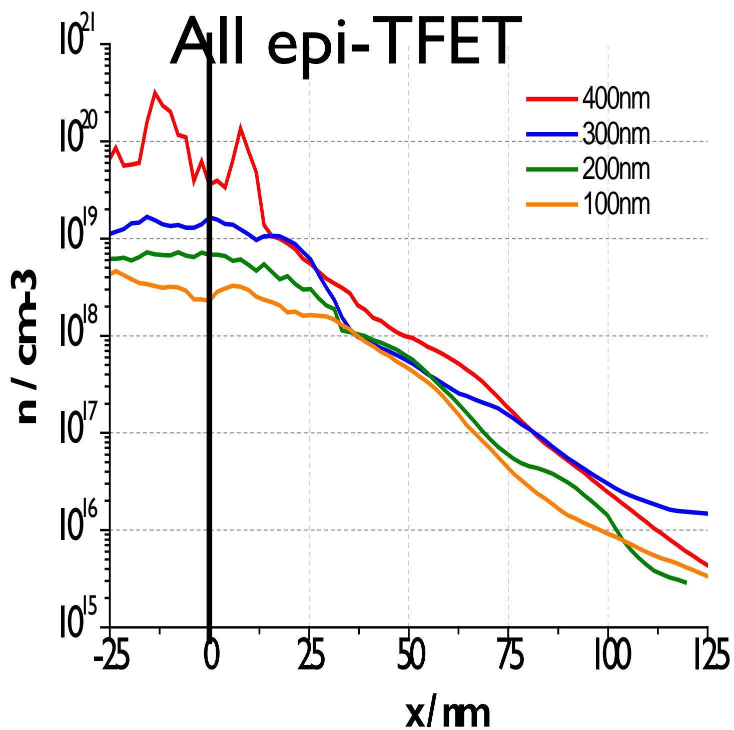


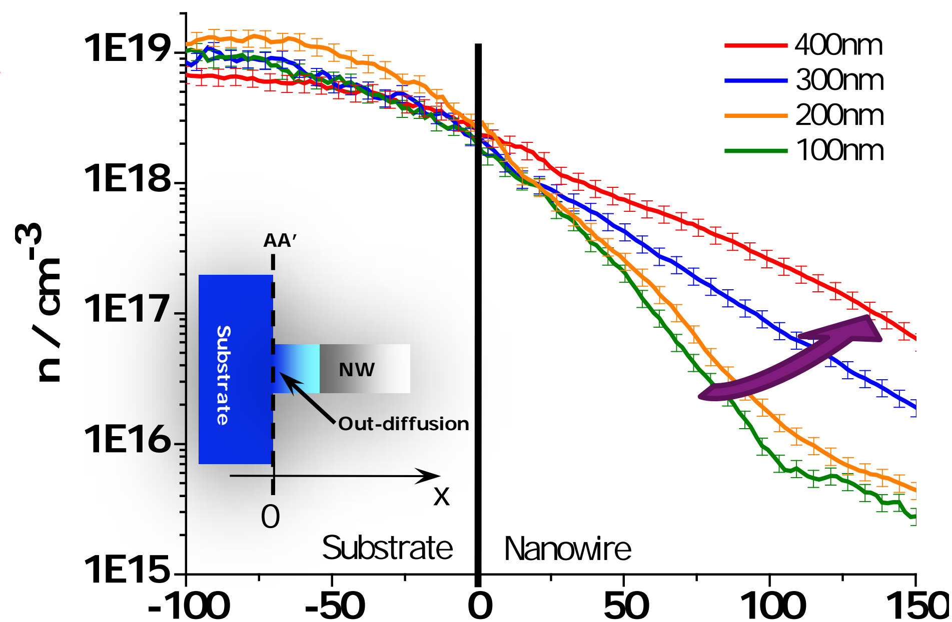






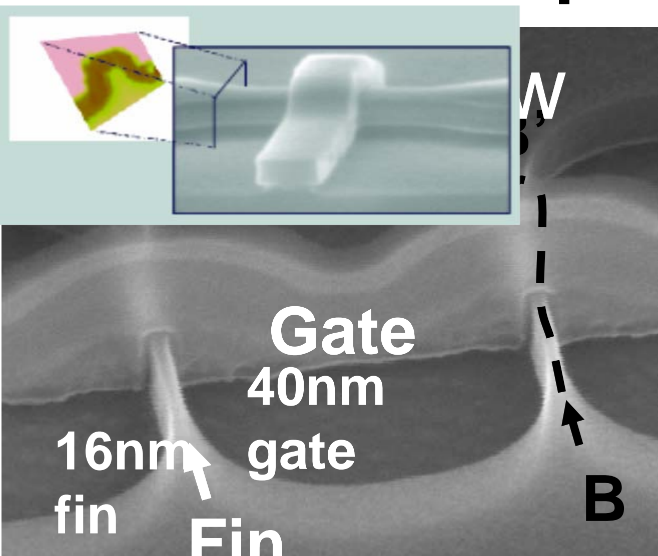


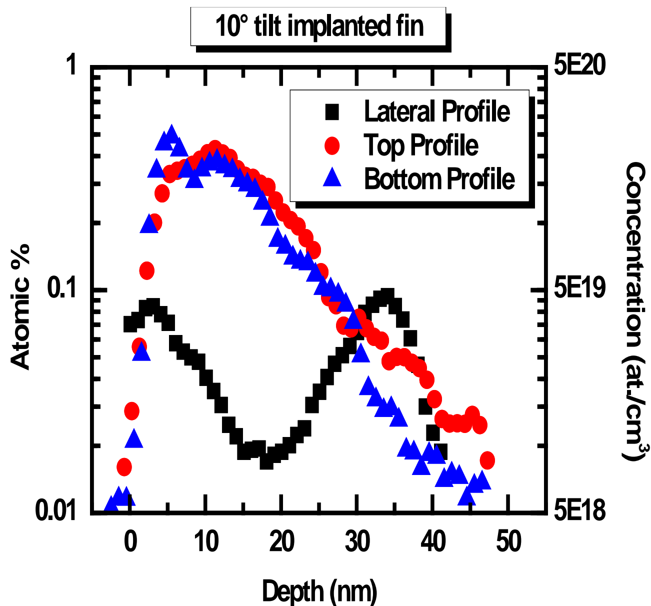


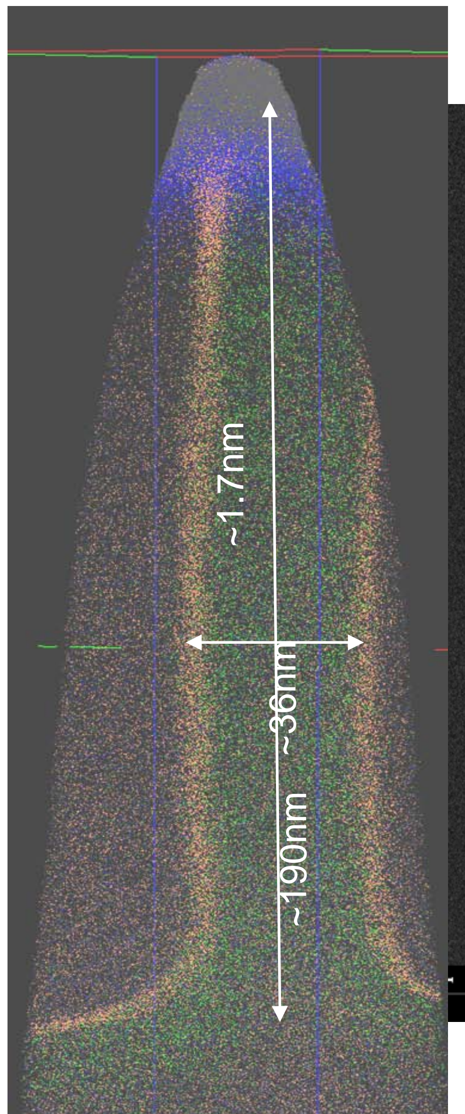


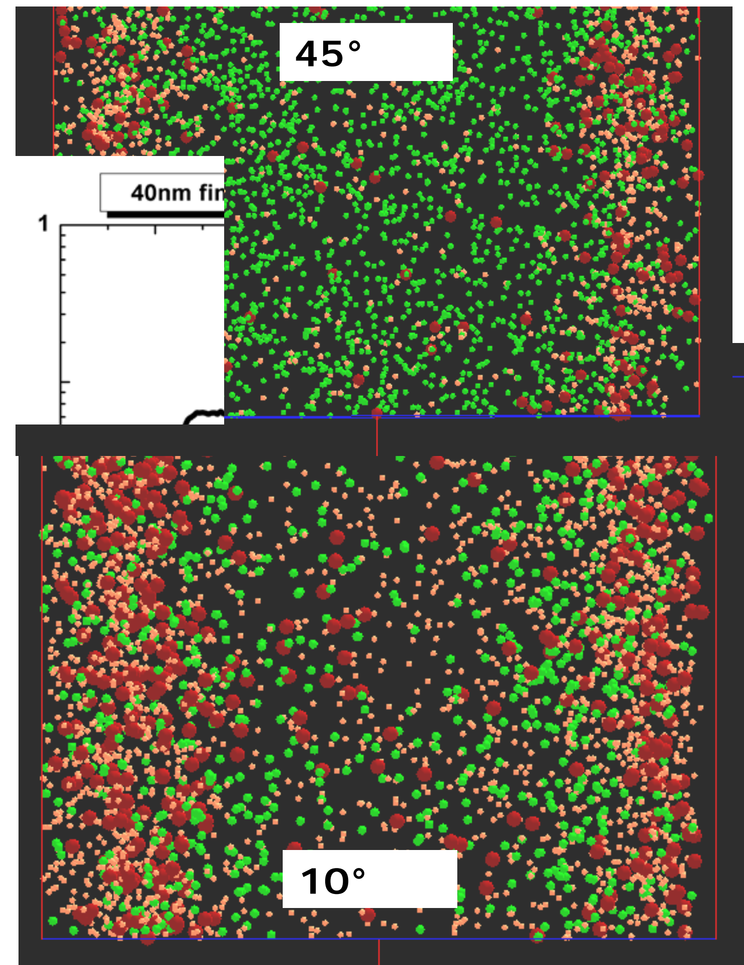
Change in Xj and gradient linked to B-implant!

Conformal doping of FIN by I/I:









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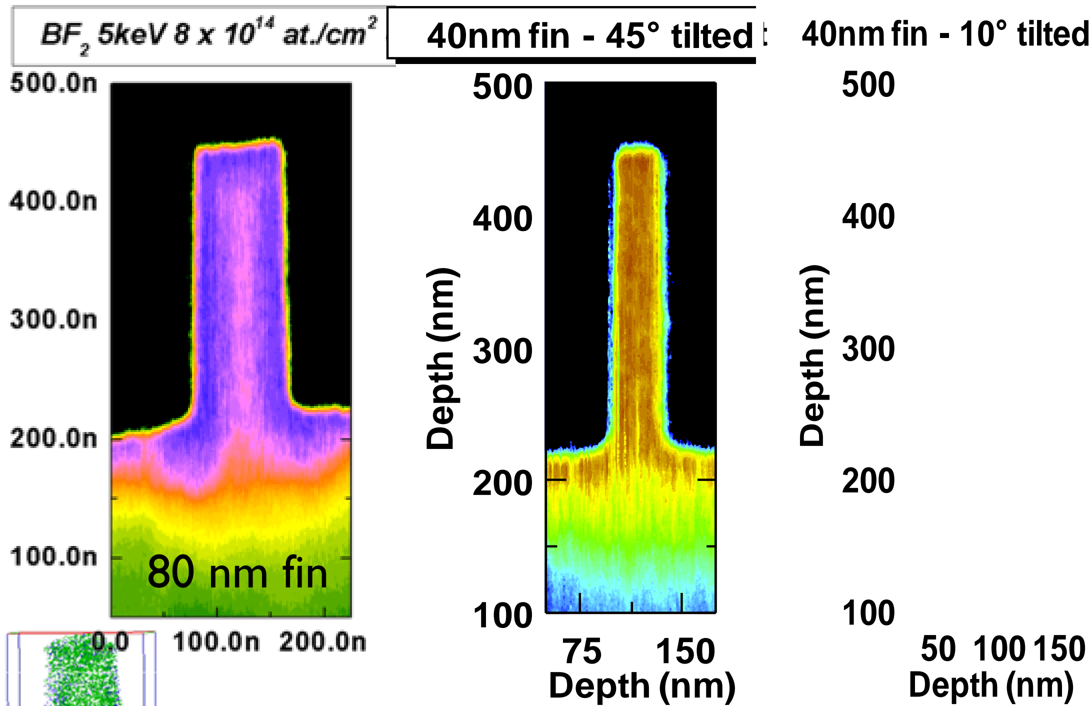
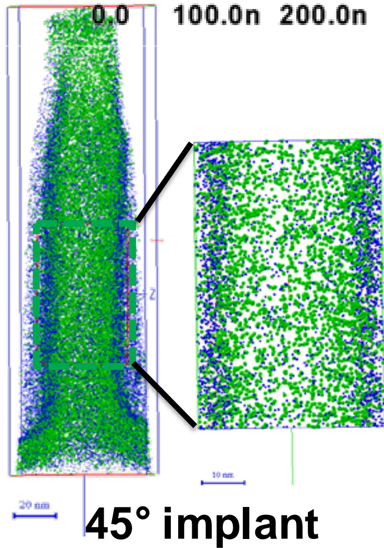
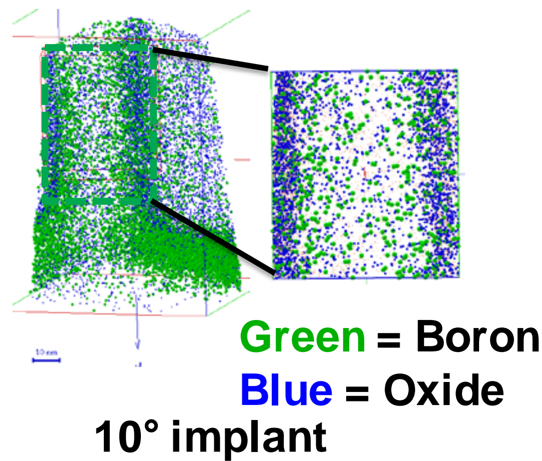
Conformality : Dopants vs Carriers





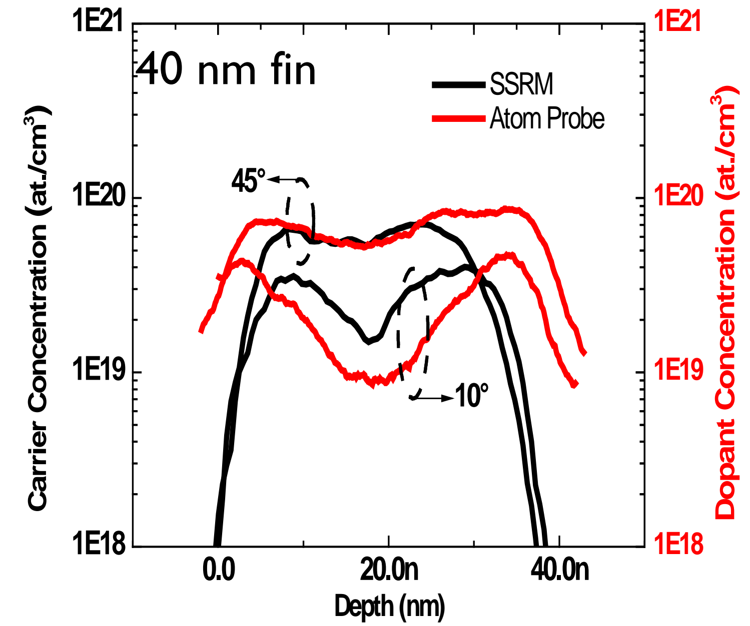
45° implant



10° implant

Green = Boron
Blue = Oxide

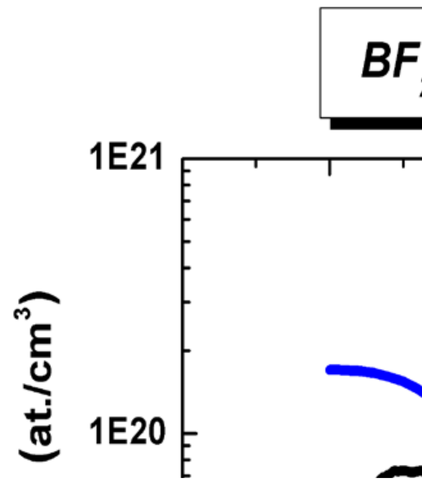
Sidewall Activation



	Conformality (Sidewall/top) (%)	Conformality (Sidewall/top) (%)
Retained dopants	45° tilted implant	10° tilted implant
Theoretical Model [10]	46	7.5
Atom Probe (APT)	39	12.5
SIMS	36	9
Active percentage of dopants		
SSRM	78	29

J.MODY , A.KAMBHAM, P.EYBEN, S.KOELLING,M.GILBERT, and W.VANDERVORST, VLSI 2010 AND IWJT-2011

Experimental vs Simulated Diffusion in FinFet



OUTLINE

1. Enhanced Metrology : PMOR

   From I/I SPC to non-contact carrier profiling in 10 micron area.

2. Material/process fundamental understanding through enhanced metrology

   A. Dopants/carriers

      i. *2D ⟺ device modeling*

      ii. *Finfet doping : doping approaches + metrology*

      iii. *Nanowires and dopant (de)activation*

   B. Layer growth/material interactions

      i. *Passivating Ge with Si : EXLE-SIMS*

      ii. *Metal gate high k interaction : BS C-AFM/XPS*

      iii. *AP of high k : image # reality (cfr M.Brillouet)*

      iv. *ReRam*

      v. *Looking for empty space*

      vi. *Quantitative phase analysis*

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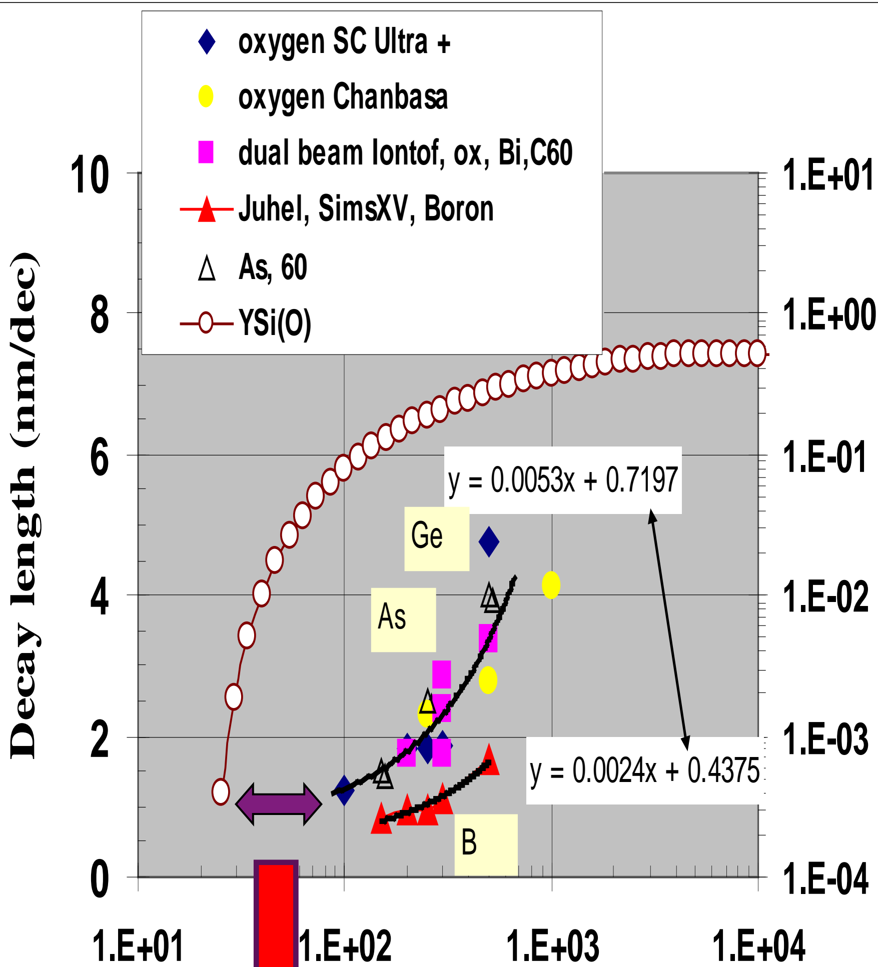
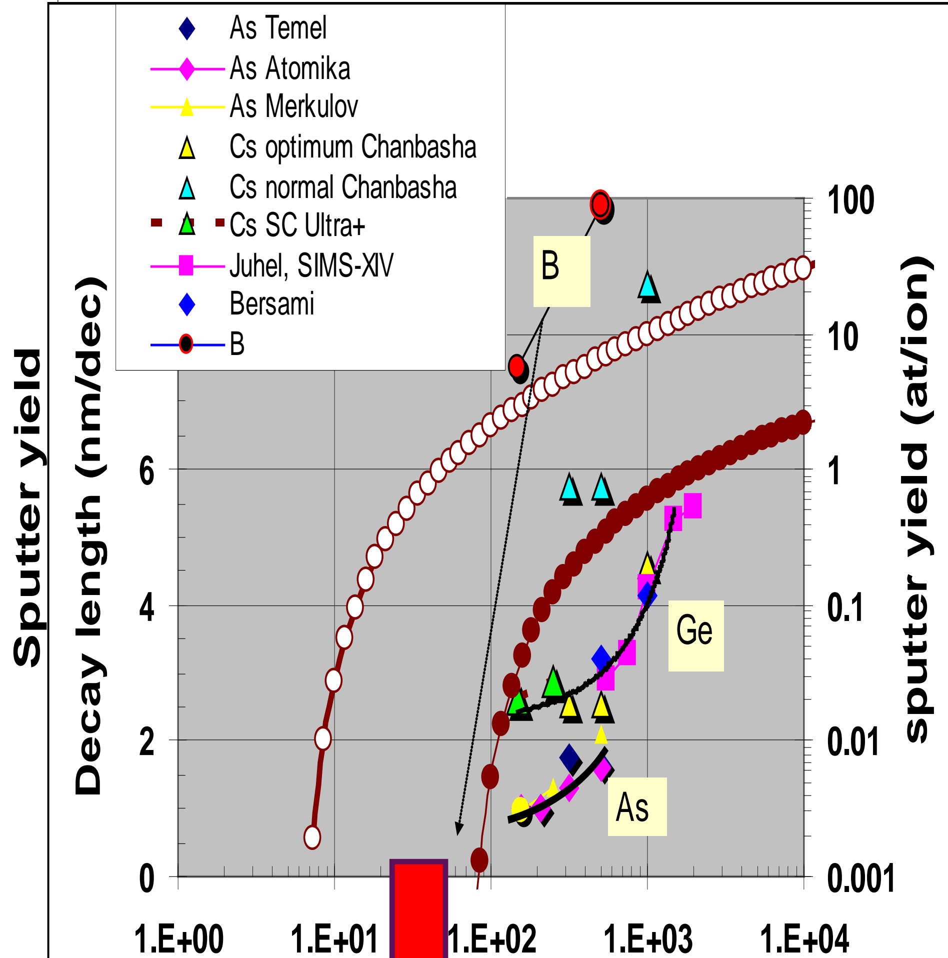
THE ULTIMATE SIMS DEPTH RESOLUTION ? EXLE-SIMS??





EXLE-SIMS : Extremely low energy SIMS

EXLE SIMS : Excellent SIMS

imec © IMEC 2010

W.Vandervorst, Applied Surface Science 255 (2008) 805-812

Improved resolution at LOW energy

Si/SiGe (3 nm)/Si

1.E+04
1.E+03
1.E+02
1.E+01
1.E+00

cts

5 7 9 11 13 15 17 19

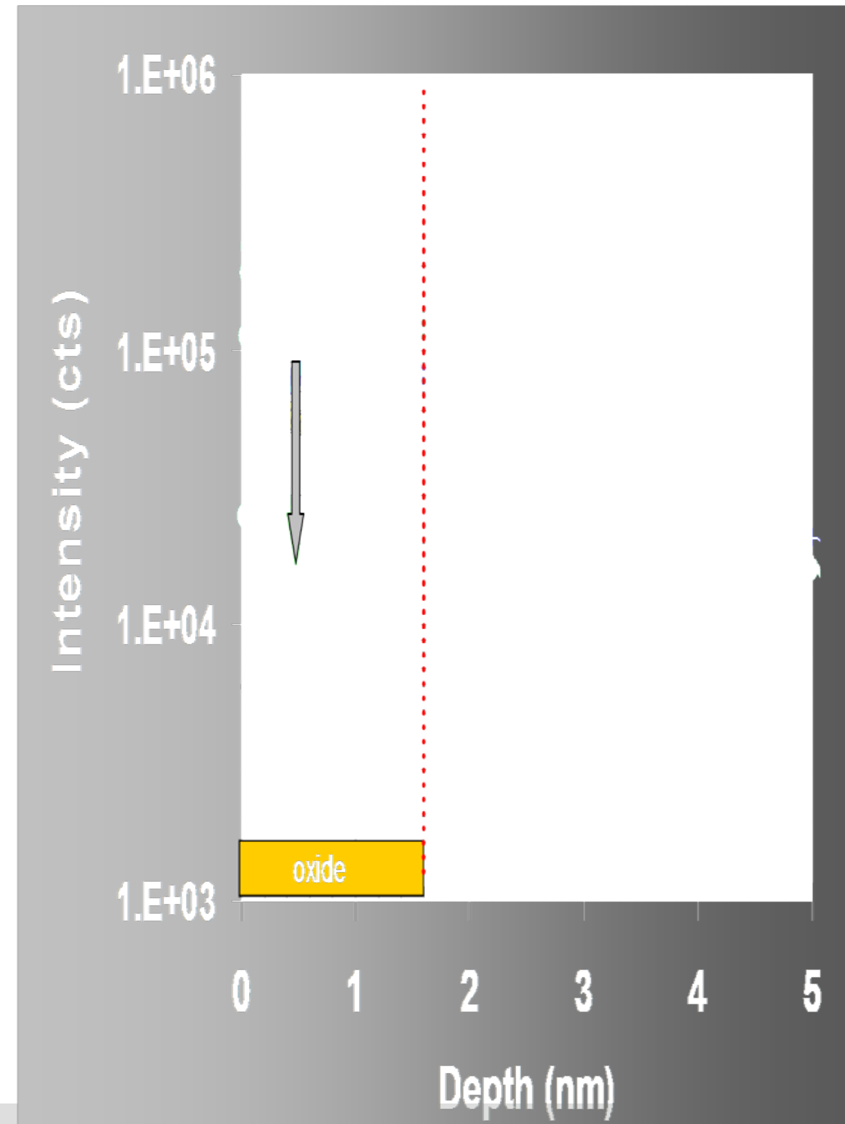
Depth (nm)

- 20keV-C60_500eV-O2,70
- 15keV-Bi3_500eV-O2
- 15keV-Bi1_500eV-O2
- 15keV-Bi1_300eV-O2.70
- 15keV-Bi3_300eV-O2,70
- 20keV-C60_300eV-O2, 70
- 15keV-Bi3_200eV-O2', 70
- O2-100 eV

0.8 nm/dec

1.2 nm/dec

B-delta in Si



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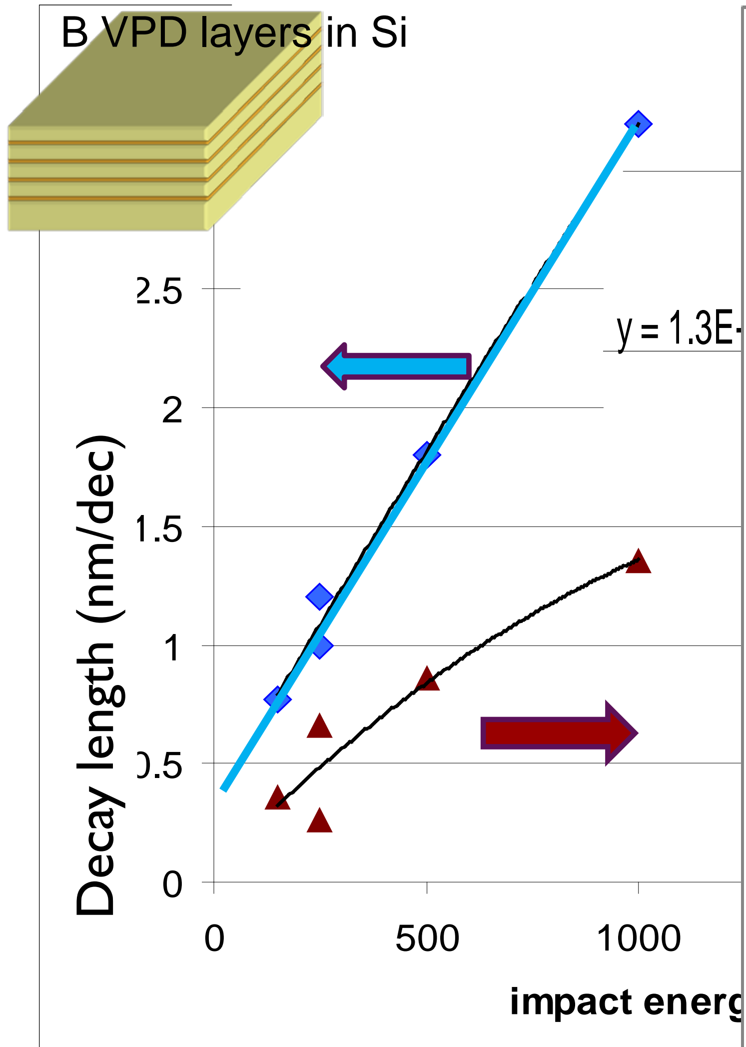
Ultimate SIMS performance : Depth Resolution And Differential shift



1E+01
1E+00
1E-01
1E-02
1E-03
1E-04
1E-05
1E-06
1E-07

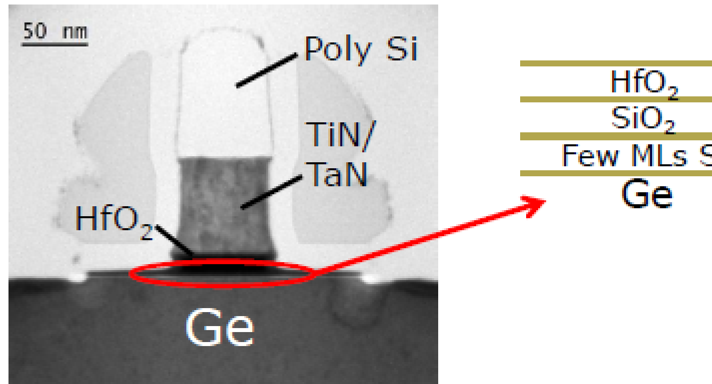
Boron intensity (au)

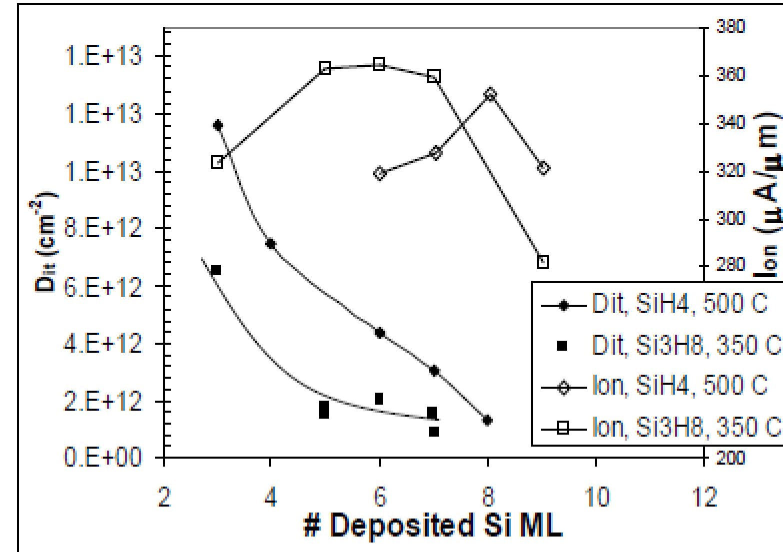
Depth (au)

1 keV
500 eV
250 eV

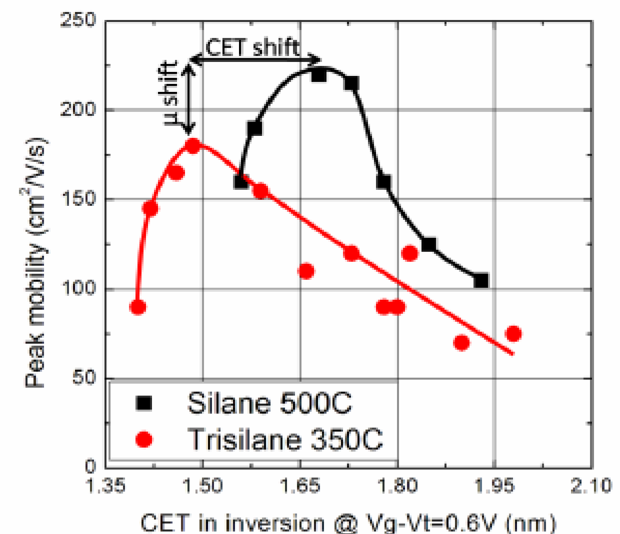
SIMS for Next generation materials : Probing Si monolayers on Ge-substrates

- Ge passivation using ultrathin (SiO_2/Si cap) interlayers to offer suitable High-K/Germanium interface quality





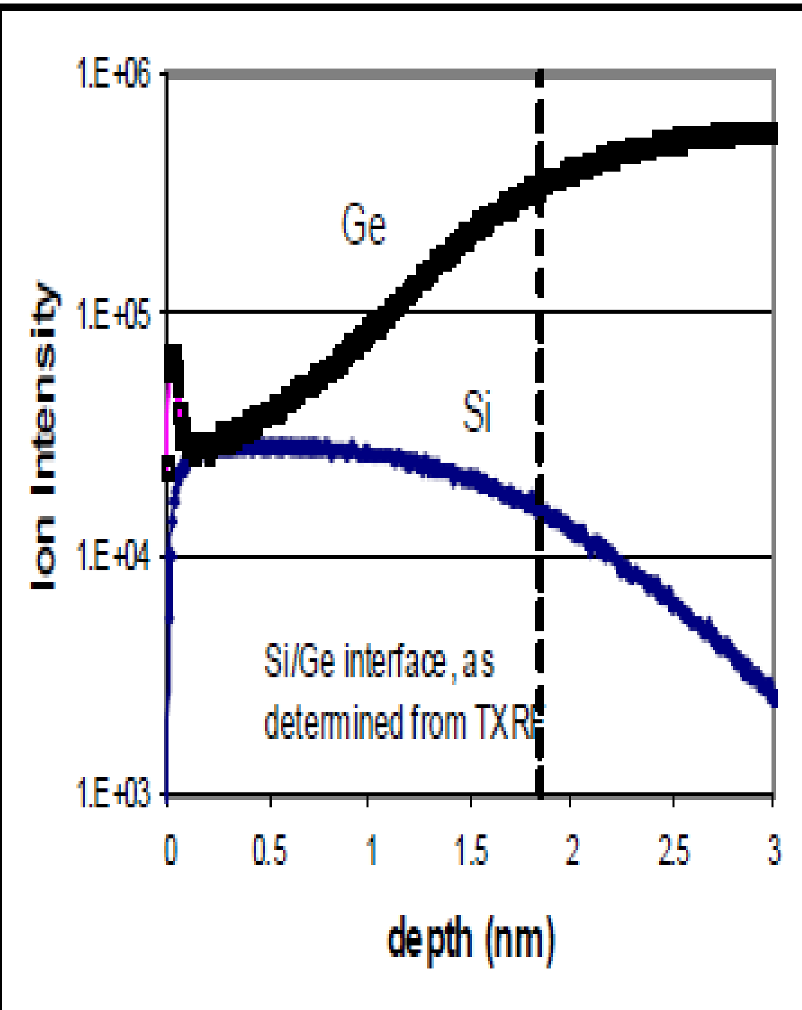
Si cap growth specifications:
- ultrathin (<10MLs [1]) to avoid strain relaxation
- Low Temperature process (<700-800°C [2]) to avoid Ge up-diffus Si cap

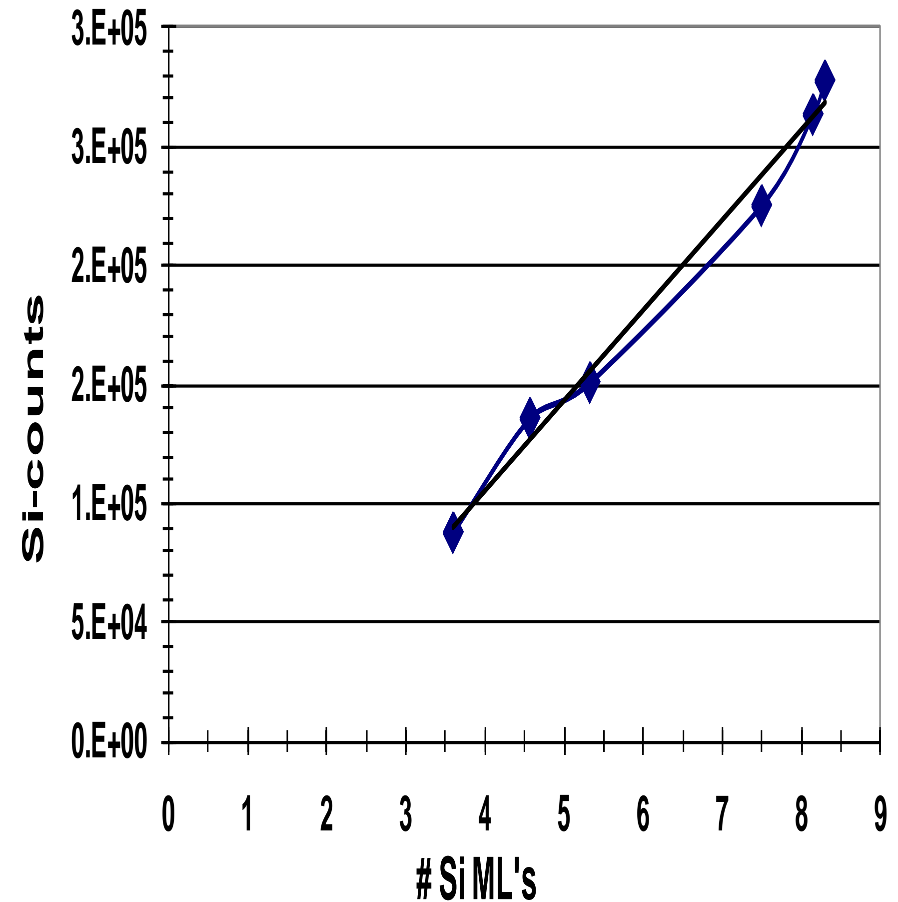


[1] Y. Fang, Thin Solid Films, 516, 2008.
[2] W. Vandervorst et al., Mat. Res. Soc. Symp. Proc. Vol. 809, 2004

SIMS challenge : measure Si-cap and potential Ge updiffusion (=cause for Dit)

EXLE-SIMS metrology at the ML scale.





Ge-segregation In Si-cap :
Gas composition dependence & Uncertainty Assessment of EXLE-Sims

Very different, must be correct

Could be SIMS

0.8 nm/dec, real or SIMS?

Much larger than "normal" transients, REAL

Si cap

SiH_4, 500C, N2, RP

Si_3H_8, 350C, N_2, ATM

10^4

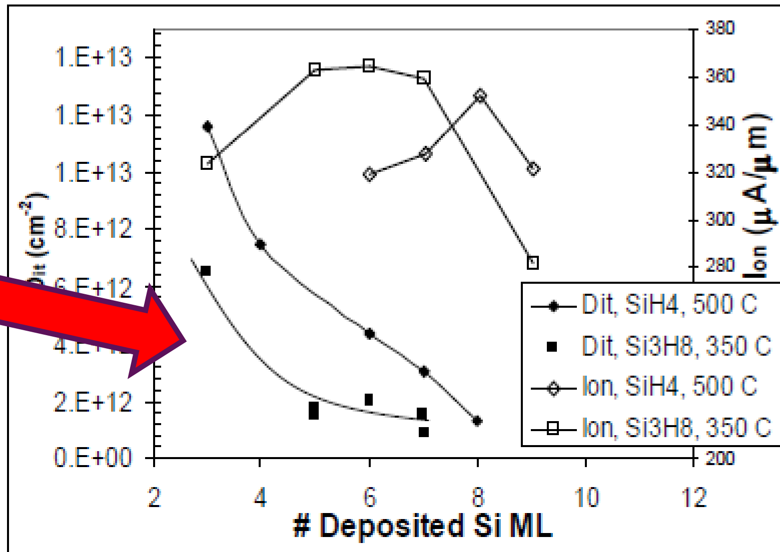
10^3

4MLs

6MLs

10MLs

SIMS depth

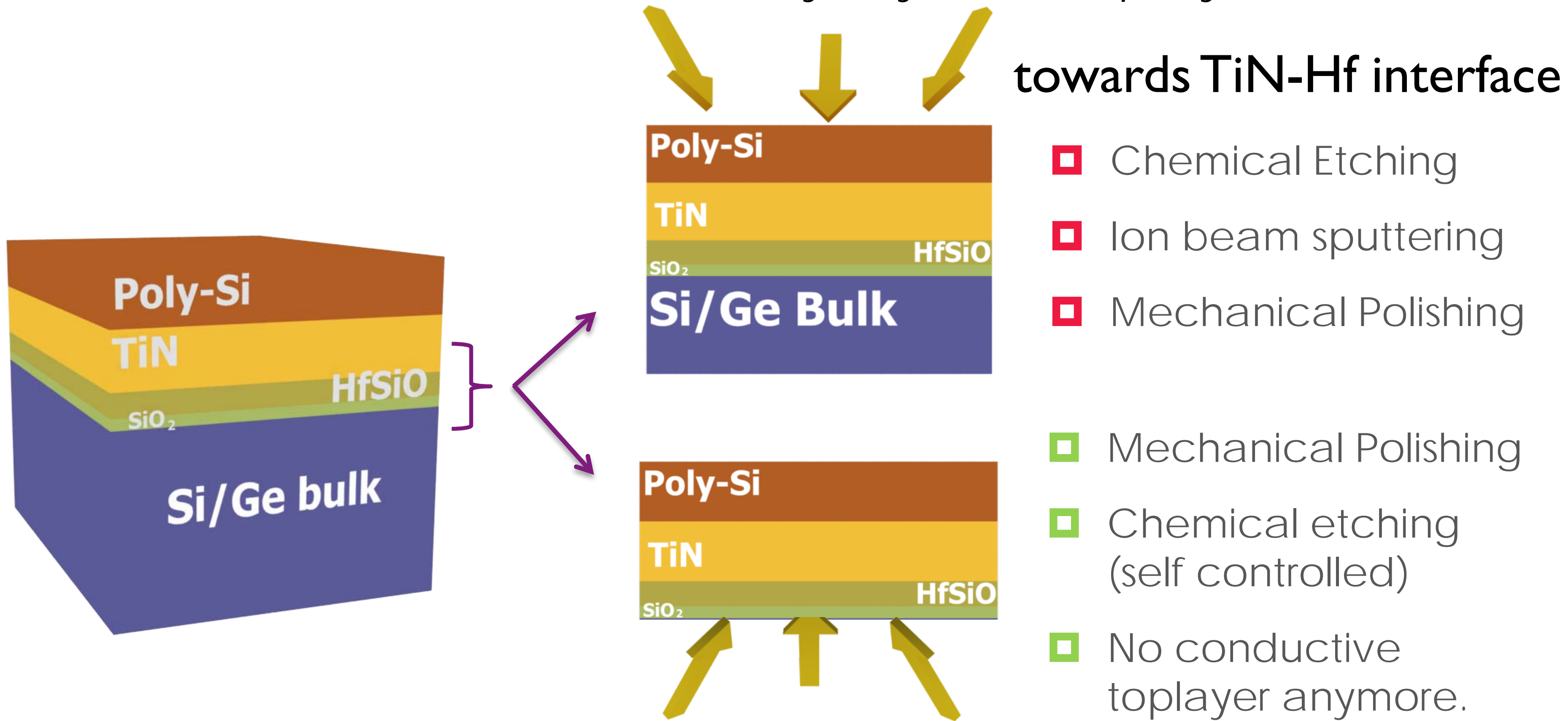


Backside Analysis : a Solution to Probe Buried Interfaces

We aim to study the buried Metal / High k interface

! XPS sampling volume too small

! C-AFM measurements shortened by any metal top layer.



towards TiN-Hf interface

- Chemical Etching
- Ion beam sputtering
- Mechanical Polishing

- Mechanical Polishing
- Chemical etching (self controlled)
- No conductive toplayer anymore.

Access to TiN-Hf interface

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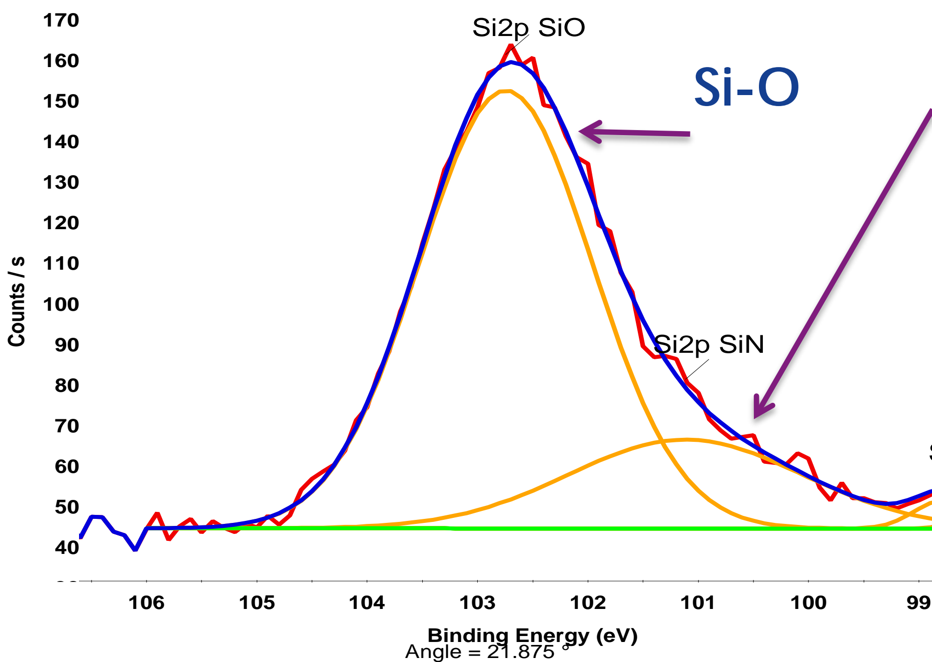
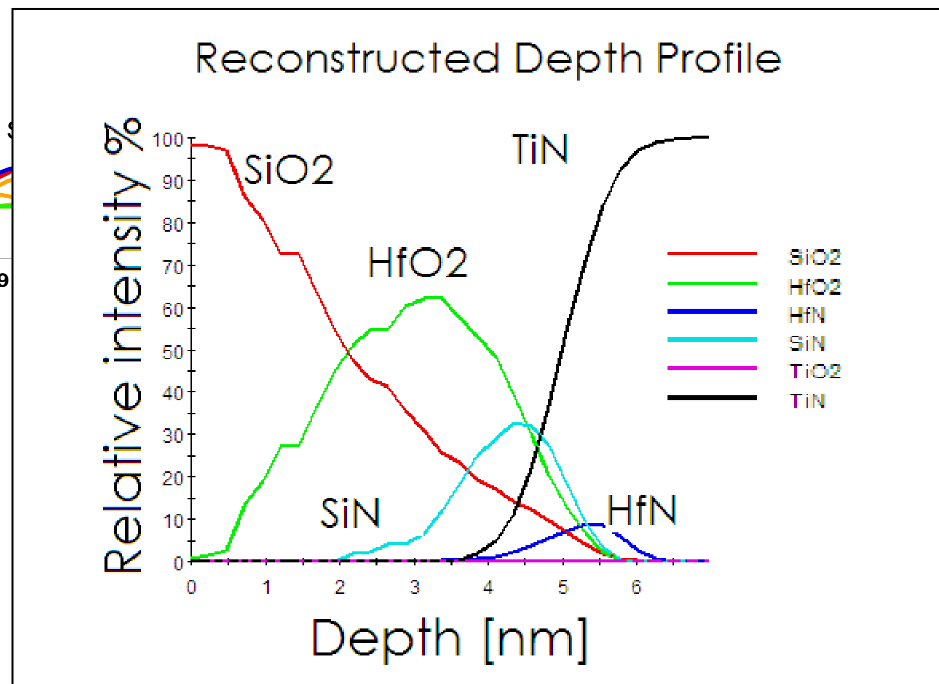
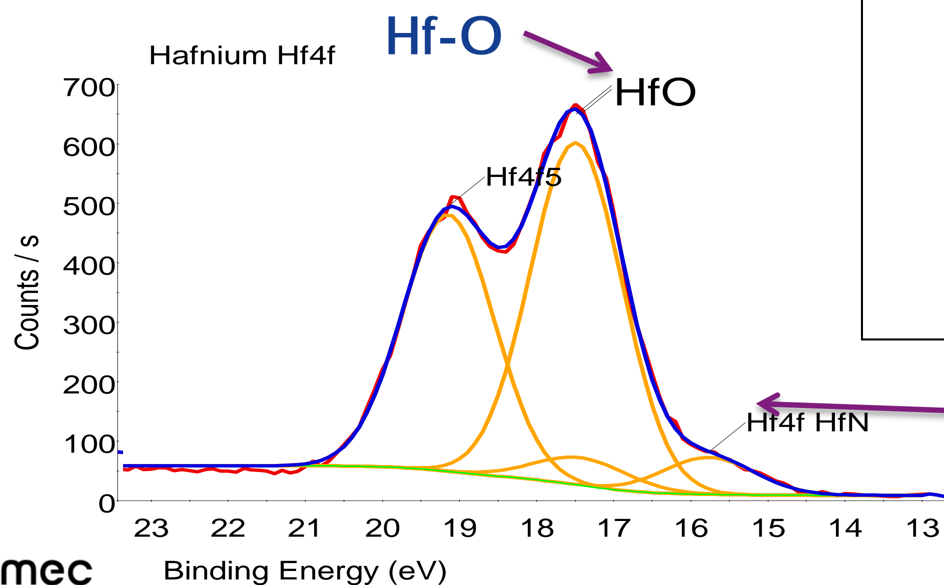
(Un)expected bondings



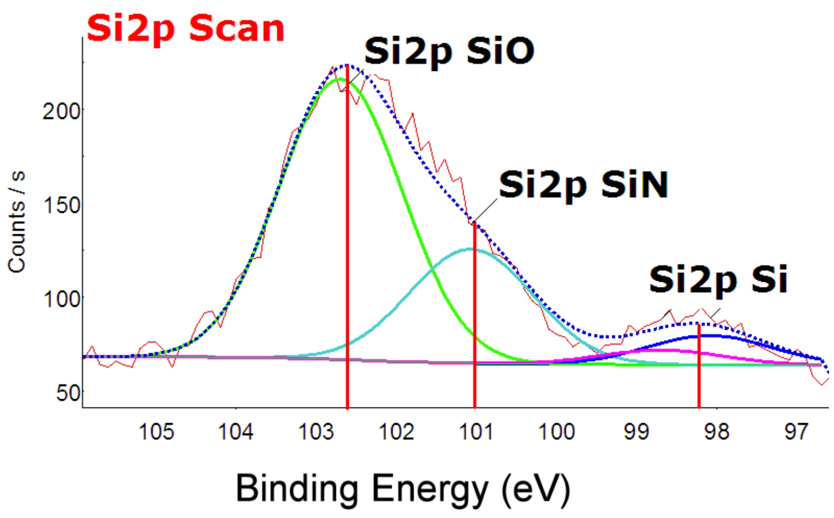


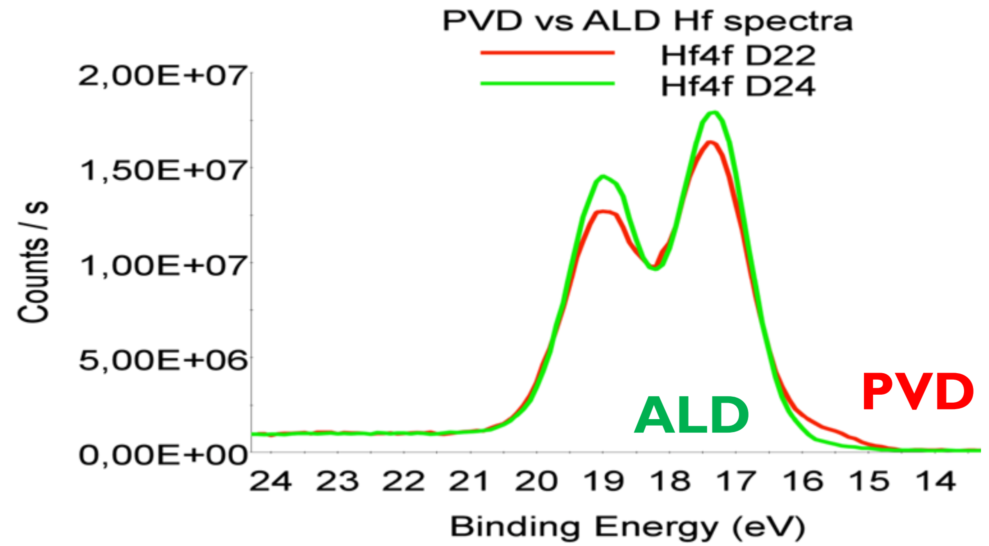


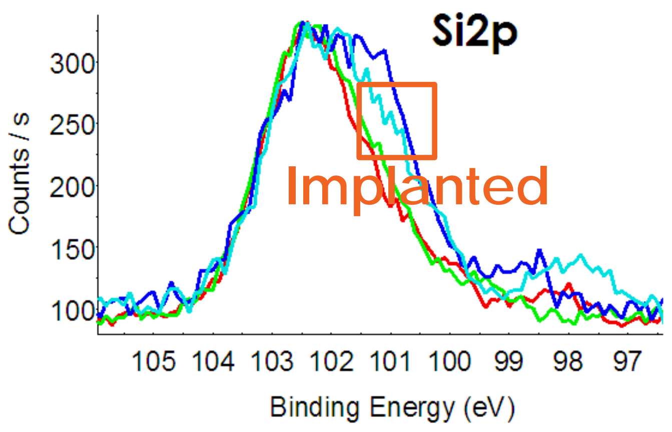
XPS SPECTRA

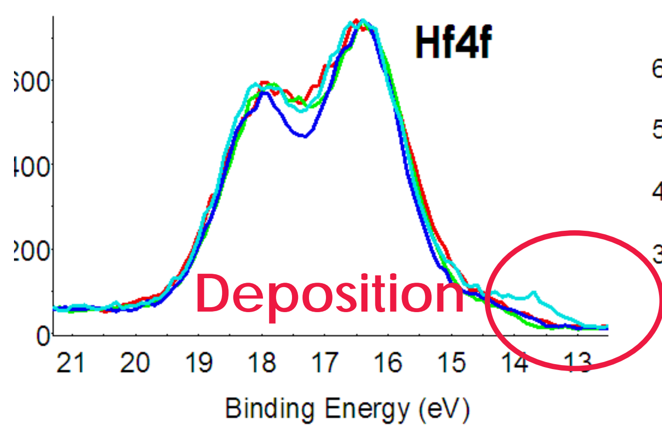
IMPACT OF IMPLANTATION

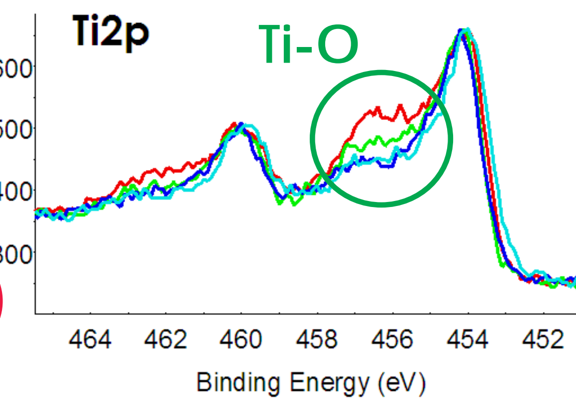
Reference
Annealing
Ann. + Argon impl.
Ann. + Arsenic impl.











S.Sahhaf, et al. ,IEEE ELECTRON DEVICE LETTERS, Vol 31, N. 4, April 2010, Vt adjustment by I/I in TiN

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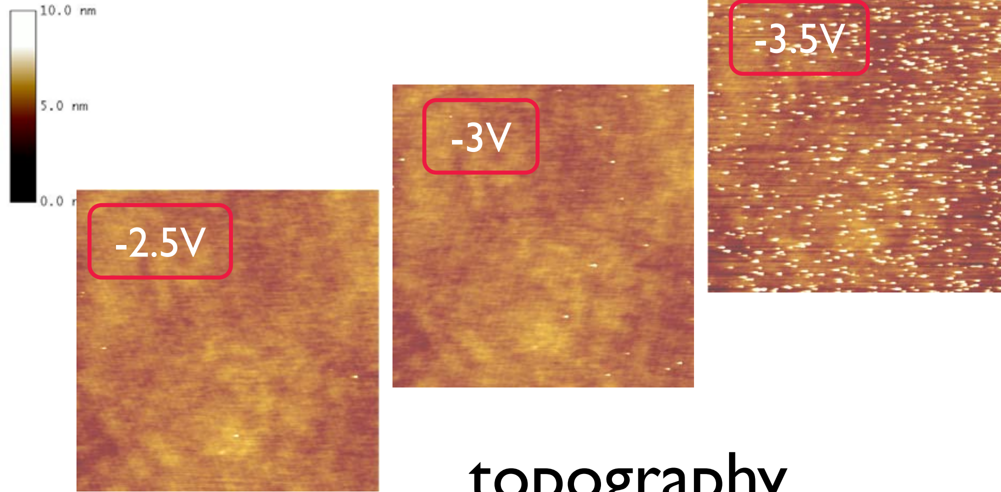
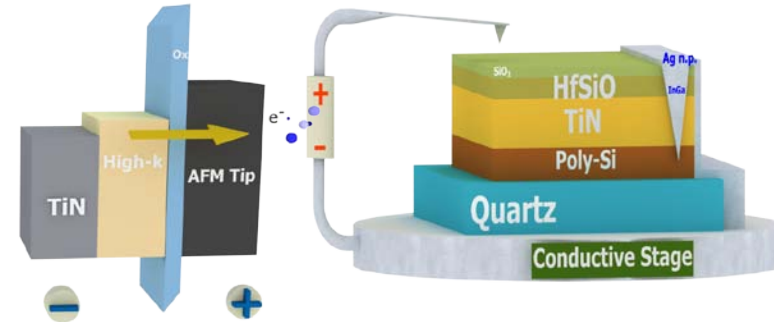
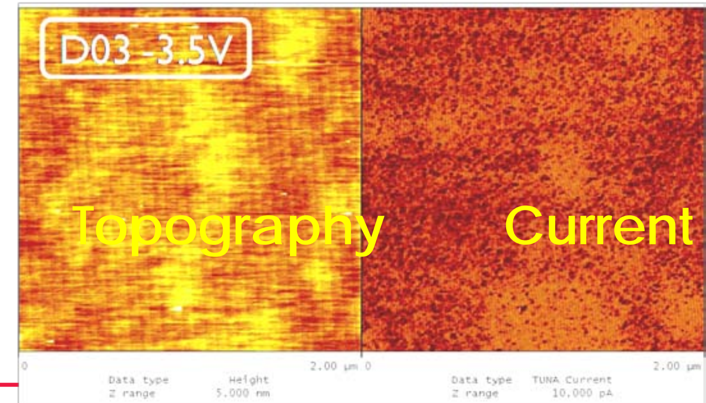
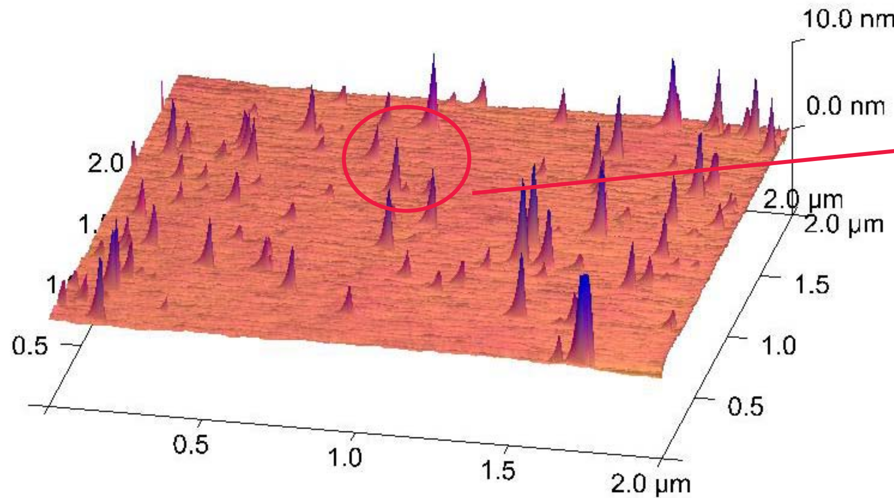
C-AFM Analysis of dielectric defects



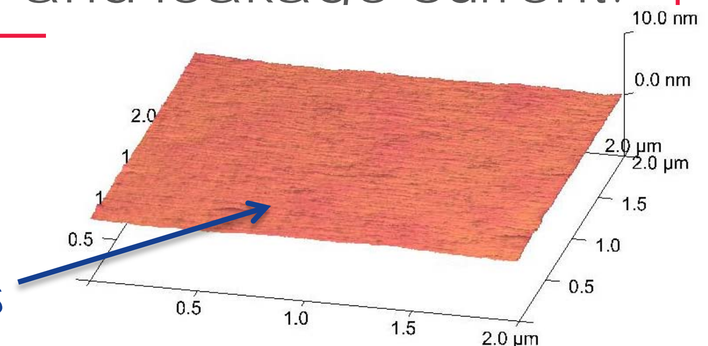
topography







Hillocks are related to breakdown positions and leakage current.



No bias

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Probing I/I Induced Defects with C-AFM Hillocks

The average hillocks height is a way to quantify leakage In C-AFM.

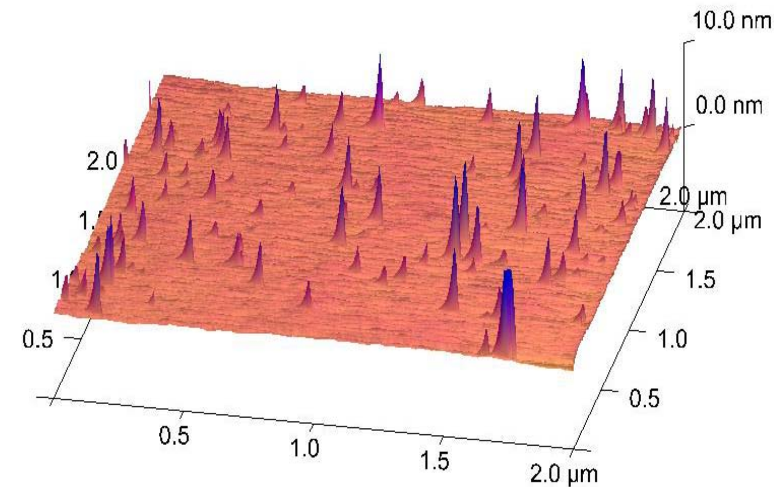
Hillocks Height vs. Voltage

D02
D03
D04
D05

Hillocks Height [nm]: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9

Voltage [V]: 1,5, 2, 2,5, 3, 3,5, 4

Implanted



Implantation increases presence low energy traps density[3]

[3] S.Sahhaf, et al. ,IEEE ELECTRON DEVICE LETTERS, Vol 31, N. 4, April 2010

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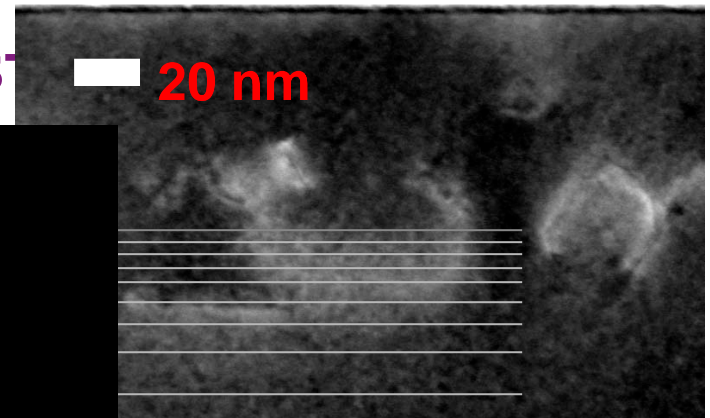
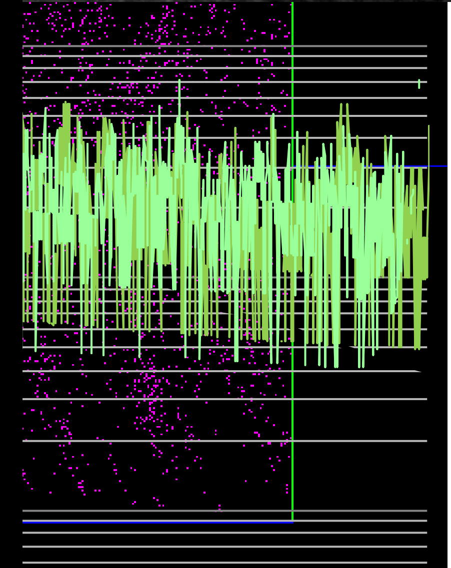
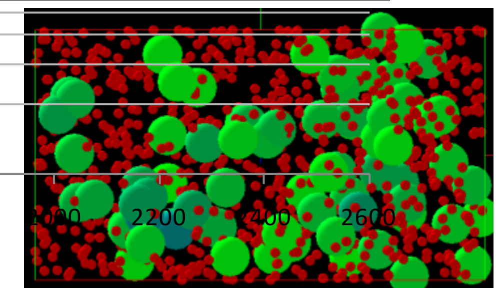
PHYSICS OF USJ FORMATION : 3D-CLUST

2.3 nm





depth in A



3.5x2.5x1.5nm
(40 B, 305 Si)

4.5x2.5x3.5nm
(72 B, 898 Si)

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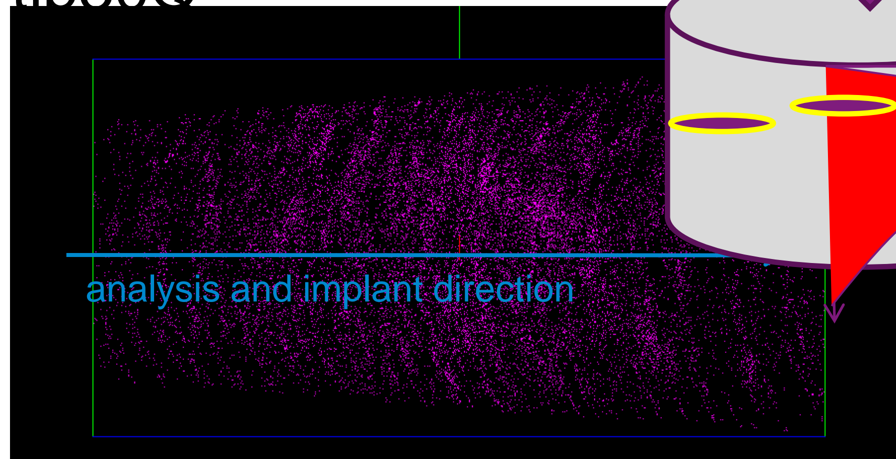
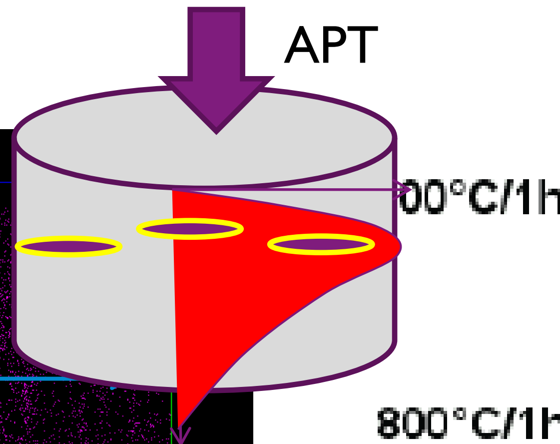
CLUSTER DISTRIBUTIONS & ARTIFACTS

B

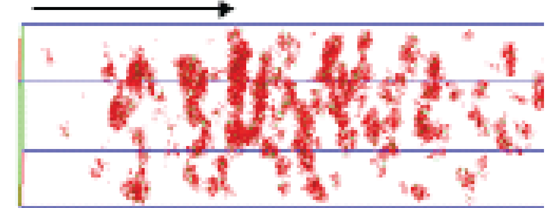
tip30Q



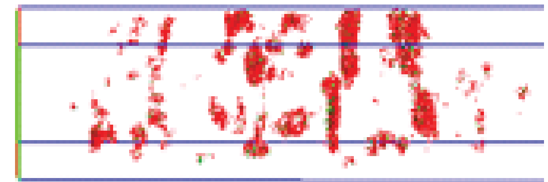


Direction d'analyse:

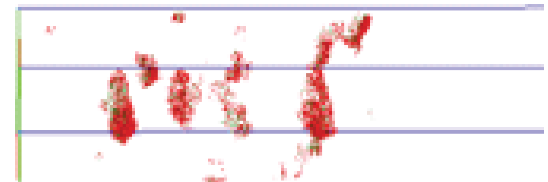
00°C/1h



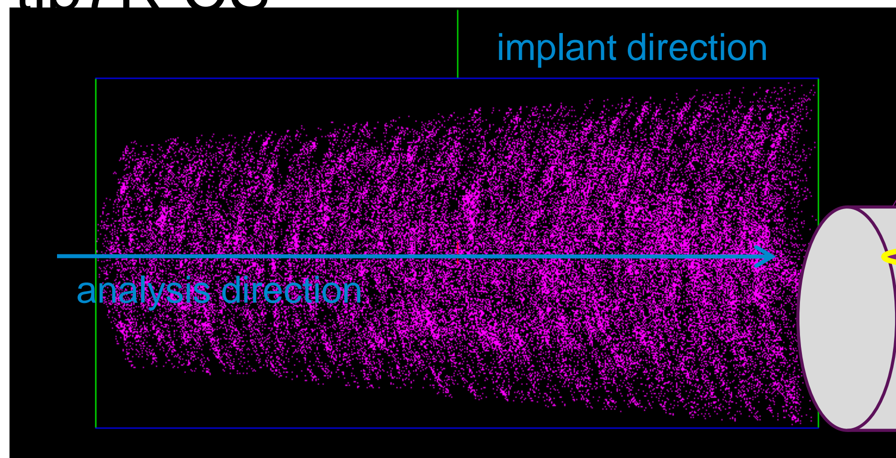
800°C/1h

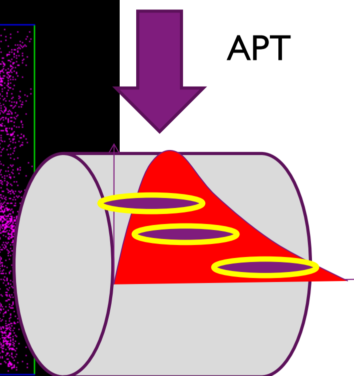


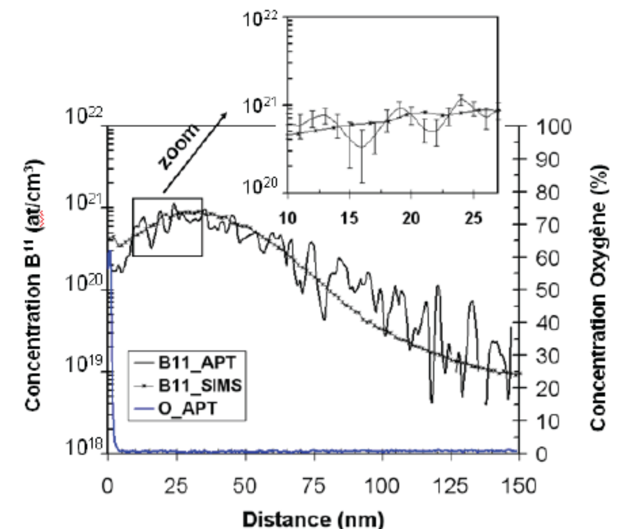
900°C/1h



tip7R CS







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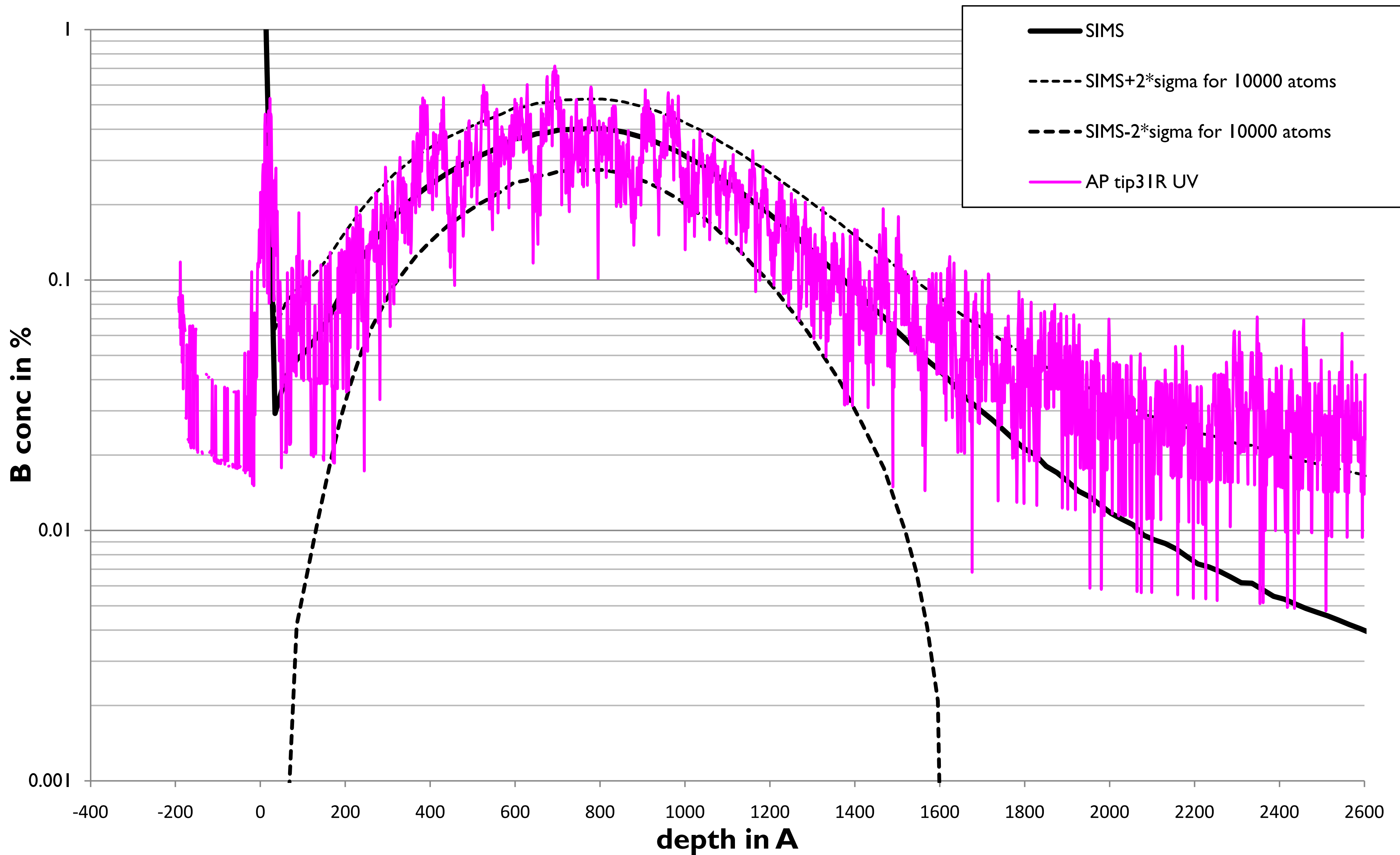
DEPTH PROFILES - BORON



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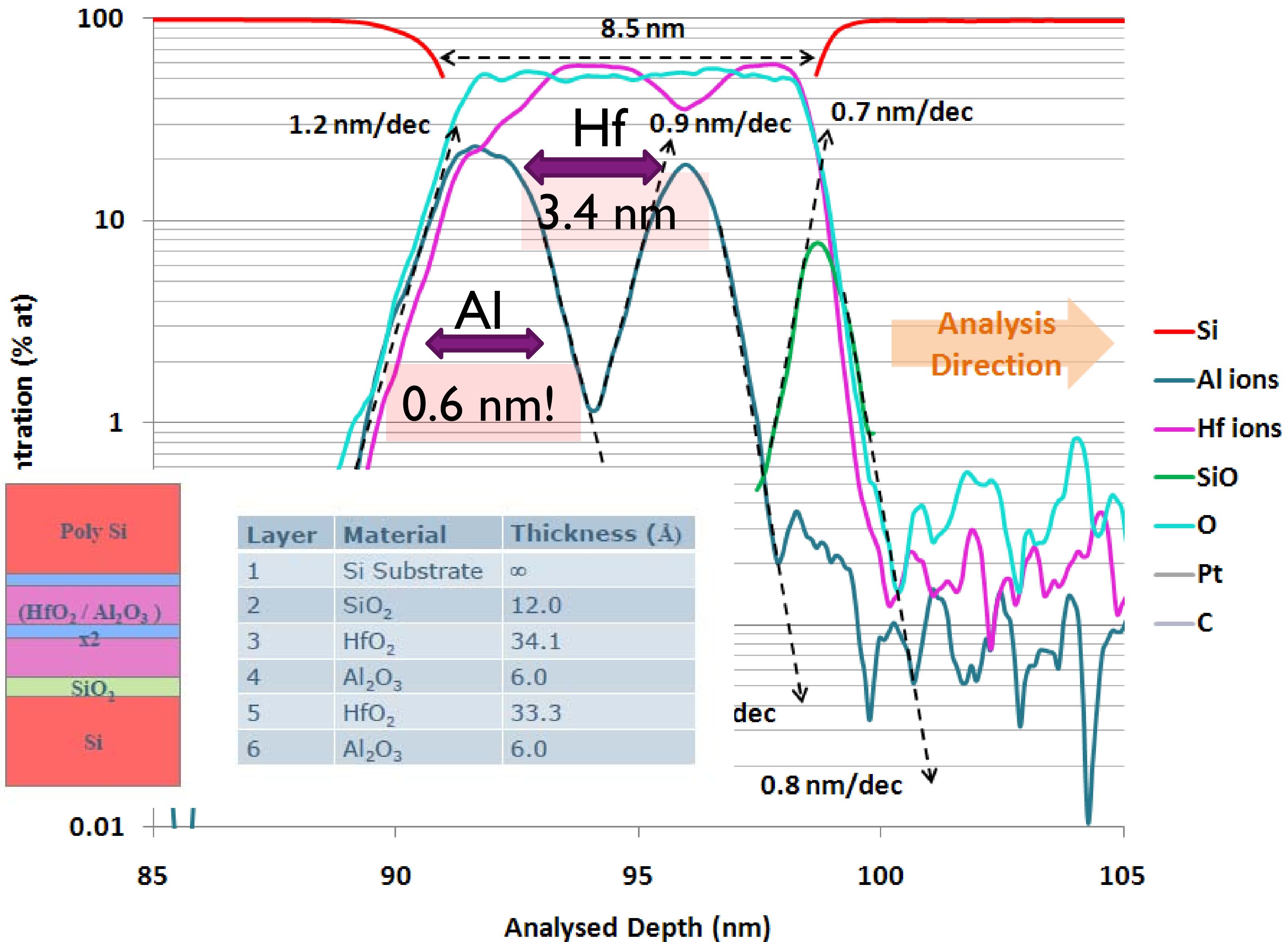
Accuracy (?) of AP-Metrology



Layer	Material	Thickness (Å)
1	Si Substrate	∞
2	SiO_2	12.0
3	HfO_2	34.1
4	Al_2O_3	6.0
5	HfO_2	33.3
6	Al_2O_3	6.0

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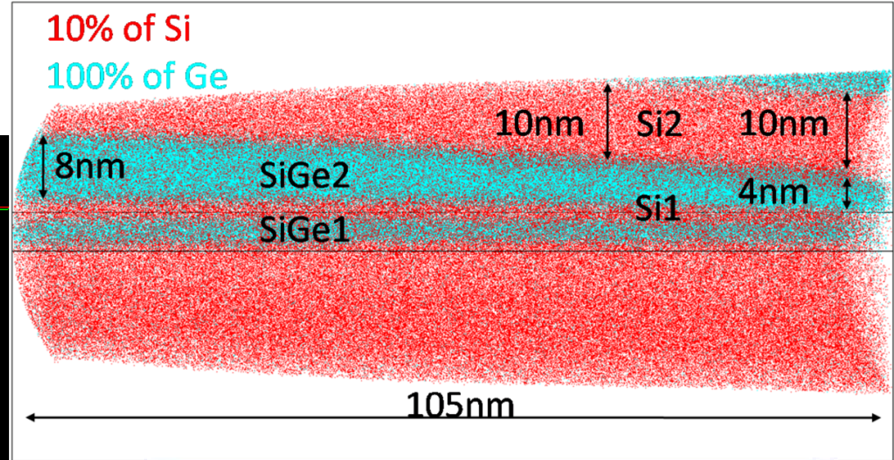
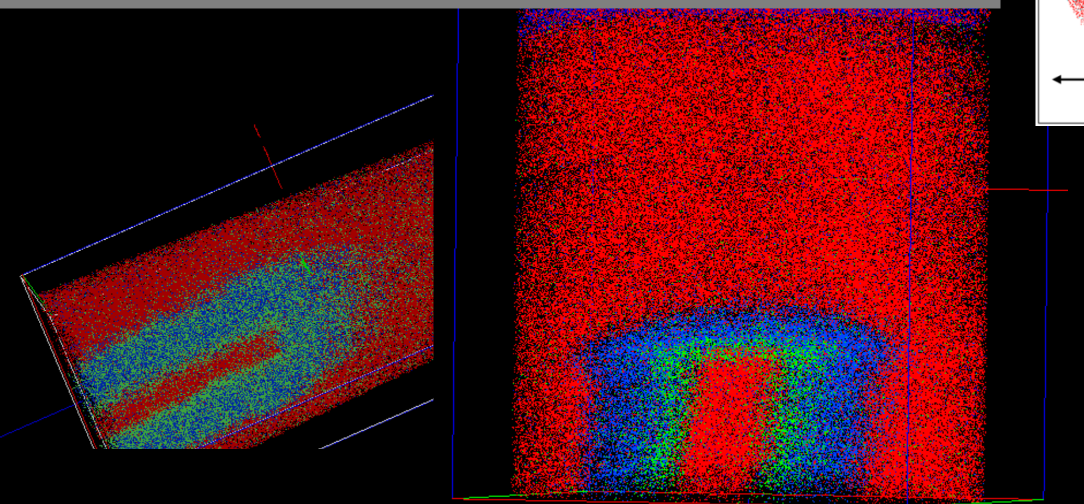
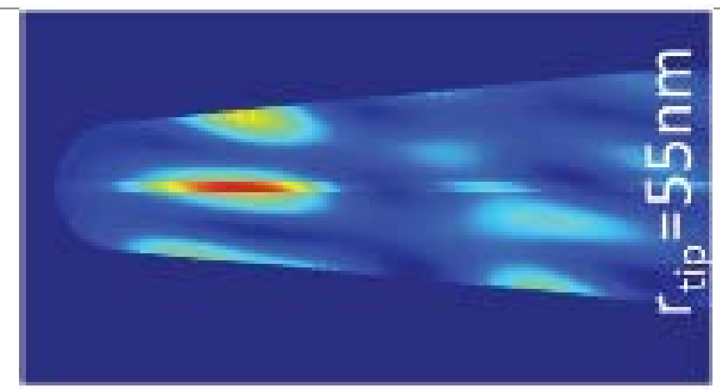
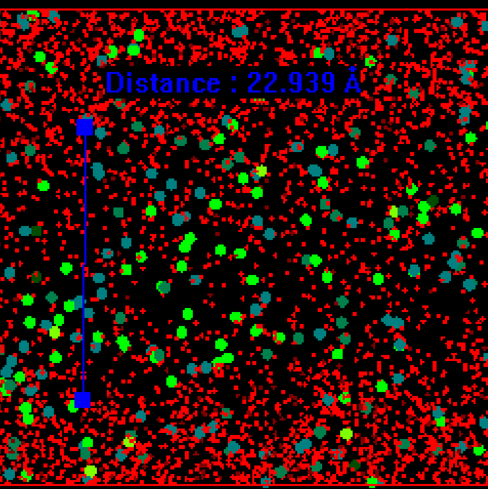
An image = distorted reality

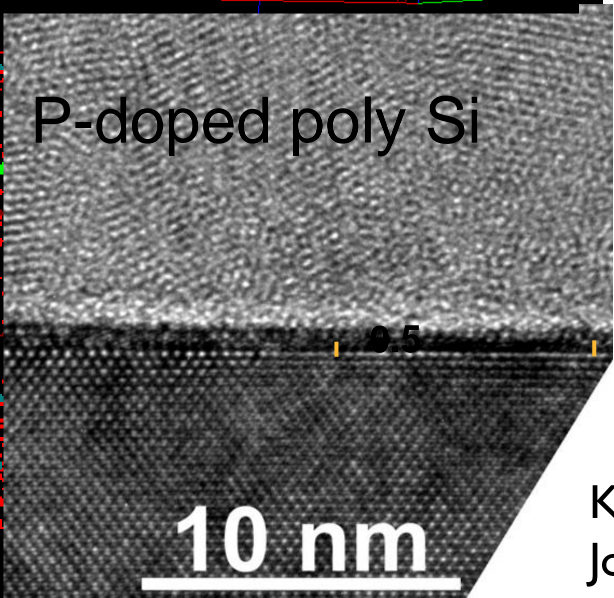
Si (30 nm), TiN (5 nm), Hf (2 nm)
Edge distortions



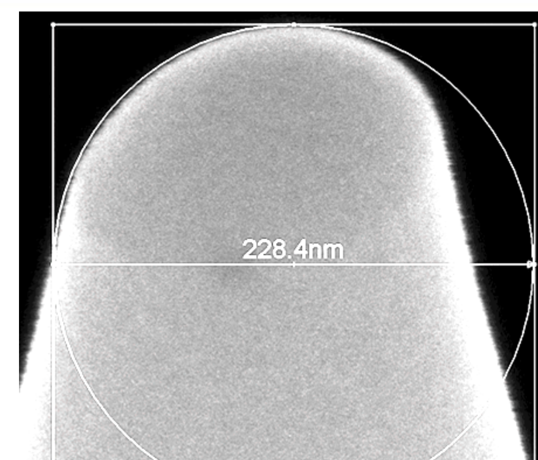








0.5



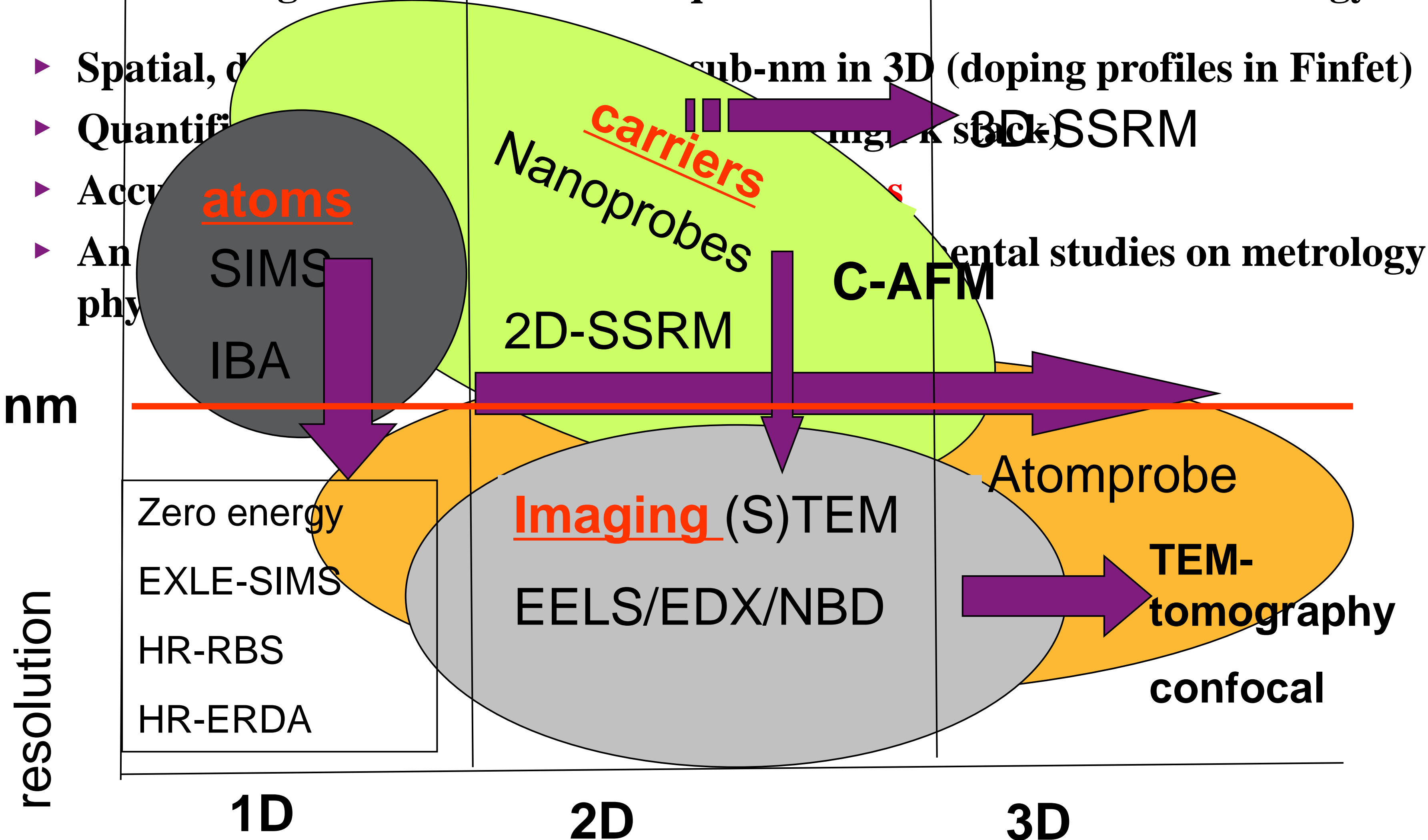
Koelling et al., Ultramicroscopy (2011)., Journ. Appl. Phys (in press)

Conclusions

Imec's Metrology Roadmap

New technologies and 3D-devices require much more advanced metrology

- **Spatial, d ... sub-nm in 3D (doping profiles in Finfet)**
- **Quantifi ... ngh-k stack)**
- **Accu ... s**
- **An ... ental studies on metrology phy**



ACKNOWLEDGEMENTS

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